M25P05

512 Kbit, Low Voltage, Serial Flash Memory With 20 MHz SPI Bus Interface

NOT FOR NEW DESIGN

FEATURES SUMMARY

This device is now designated as "Not for New Design". Please use the M25P05-A in all future designs (as described in application note AN1511).

- 512 Kbit of Flash Memory
- Page Program (up to 128 Bytes) in 3 ms (typical)
- Sector Erase (256 Kbit) in 1 s (typical)
- Bulk Erase (512 Kbit) in 2 s (typical)
- 2.7 V to 3.6 V Single Supply Voltage
- SPI Bus Compatible Serial Interface
- 20 MHz Clock Rate (maximum)
- Deep Power-down Mode 1 µA (typical)
- Electronic Signature
- More than 100,000 Erase/Program Cycles per Sector
- More than 20 Year Data Retention

Figure 1. Packages

SO8 (MN)
150 mil width

This is information on a product still in production but not recommended for new designs.

SUMMARY DESCRIPTION

The M25P05 is a 512 Kbit (64K x 8) Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

The memory can be programmed 1 to 128 bytes at a time, using the Page Program instruction.

The memory is organized as 2 sectors, each containing 256 pages. Each page is 128 bytes wide. Thus, the whole memory can be viewed as consisting of 512 pages, or 65536 bytes.

The whole memory can be erased using the Bulk Erase instruction, or a sector at a time, using the Sector Erase instruction.

Figure 2. Logic Diagram

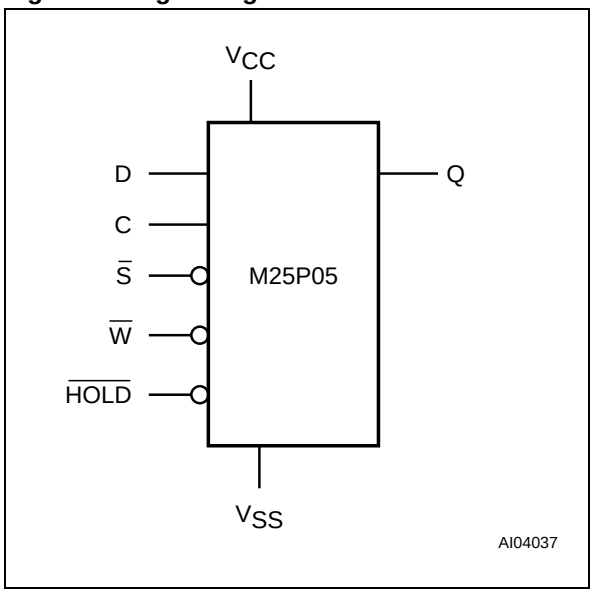
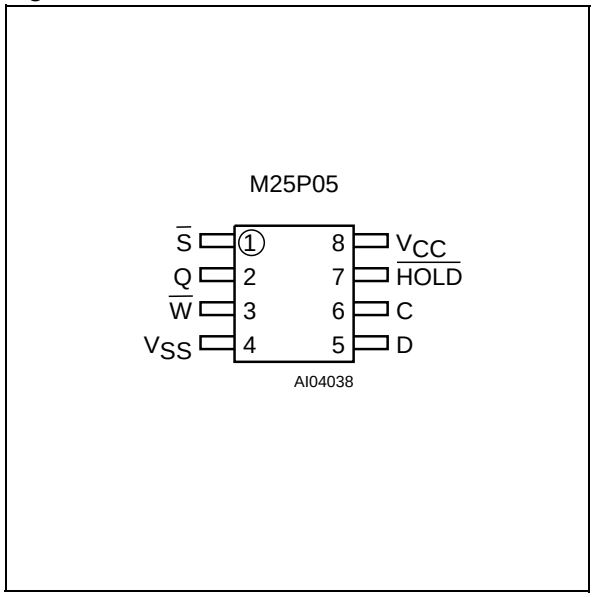


Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 3. SO Connections



SIGNAL DESCRIPTION

Serial Data Output (Q). This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

Serial Data Input (D). This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

Serial Clock (C). This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

Chip Select ($\overline{S}$). When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

Hold ($\overline{HOLD}$). The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

Write Protect ($\overline{W}$). The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

SPI MODES

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

– CPOL=0, CPHA=0

– CPOL=1, CPHA=1

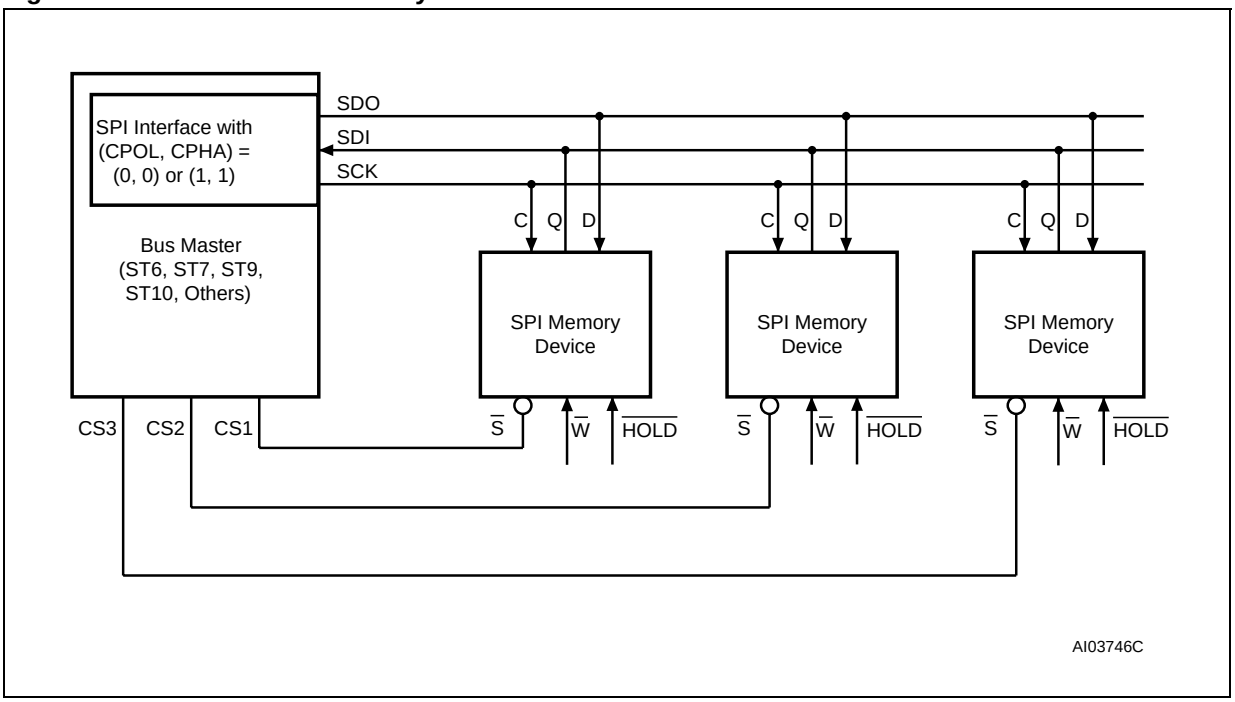
For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 5, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

– C remains at 0 for (CPOL=0, CPHA=0)

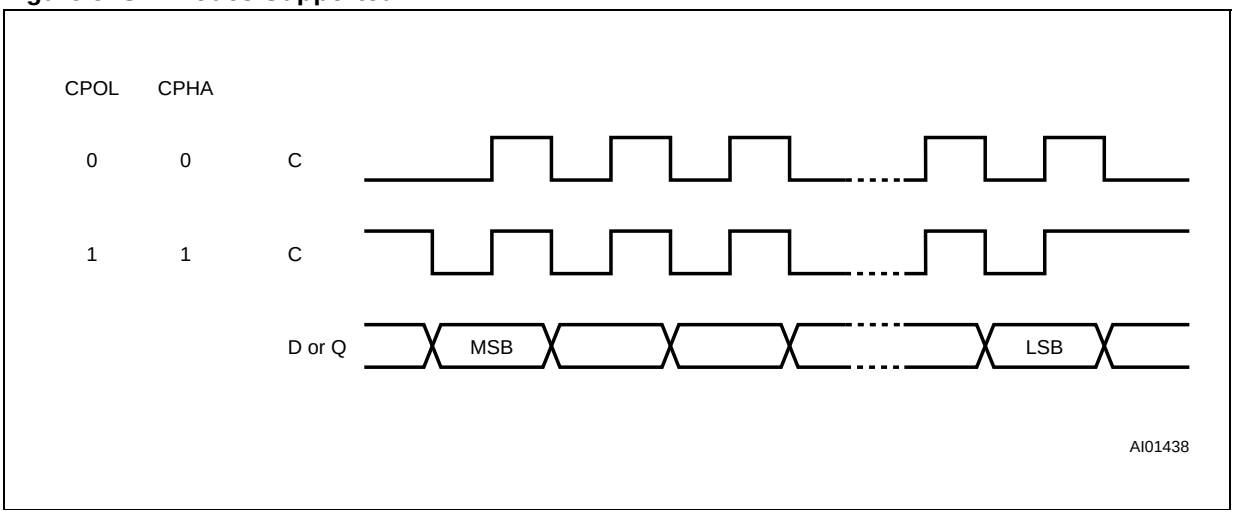
– C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. Bus Master and Memory Devices on the SPI Bus



Note: 1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 5. SPI Modes Supported



OPERATING FEATURES

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 128 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase and Bulk Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a sector at a time, using the Sector Erase (SE) instruction, or throughout the entire memory, using the Bulk Erase (BE) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, or t_{BE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select ($\overline{S}$) is Low, the device is enabled, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Stand-by Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Electronic Signature (RES) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertant Write, Program or Erase instructions.

Status Register

The Status Register contains a number of status and control bits, as shown in Table 5, that can be read or set (as appropriate) by specific instructions.

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP1, BP0 bits. The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

SRWD bit. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits.

Table 2. Protected Area Sizes

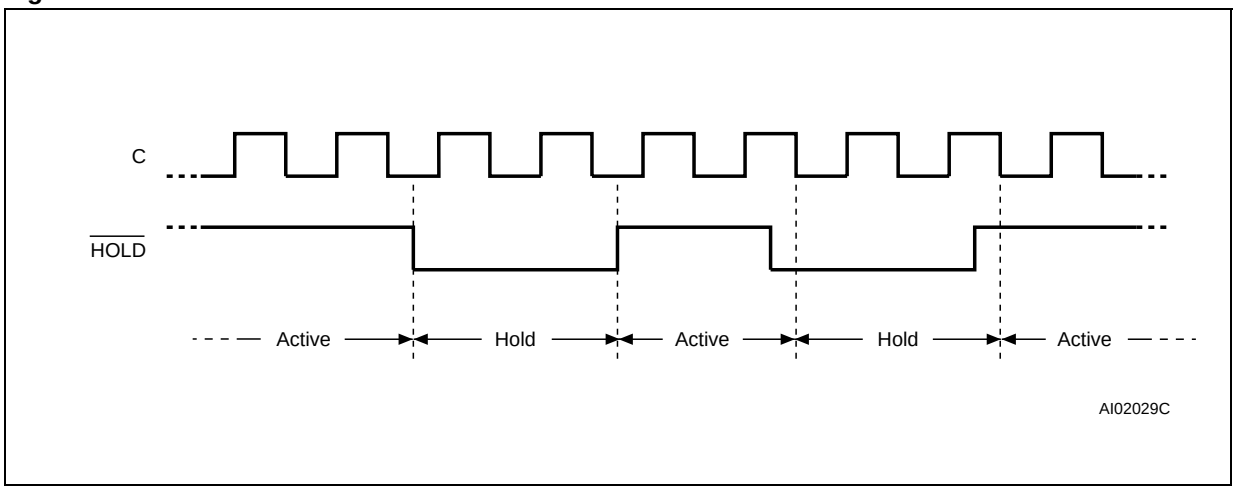
Status Register Content		Memory Content	
BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	none	All sectors (Sectors 0 and 1)
0	1	No protection against Page Program (PP) and Sector Erase (SE) All sectors (Sectors 0 and 1) protected against Bulk Erase (BE)	
1	0		
1	1	All sectors (Sectors 0 and 1)	none

Protection Modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25P05 boasts the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertant changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit . This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- The Block Protect (BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect ($\overline{W}$) signal, in co-operation with the Status Register Write Disable (SRWD) bit, allows the Block Protect (BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be write-protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertant Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Figure 6. Hold Condition Activation



Hold Condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

The Hold condition starts on the falling edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in Figure 6).

The Hold condition ends on the rising edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low.

If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts when Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends when Serial Clock (C) next goes Low. (This is shown in Figure 6).

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

Normally, the device is kept selected, with Chip Select ($\overline{S}$) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select ($\overline{S}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{HOLD}$) High, and then to drive Chip Select ($\overline{S}$) Low. This prevents the device from going back to the Hold condition.

MEMORY ORGANIZATION

The memory is organized as:

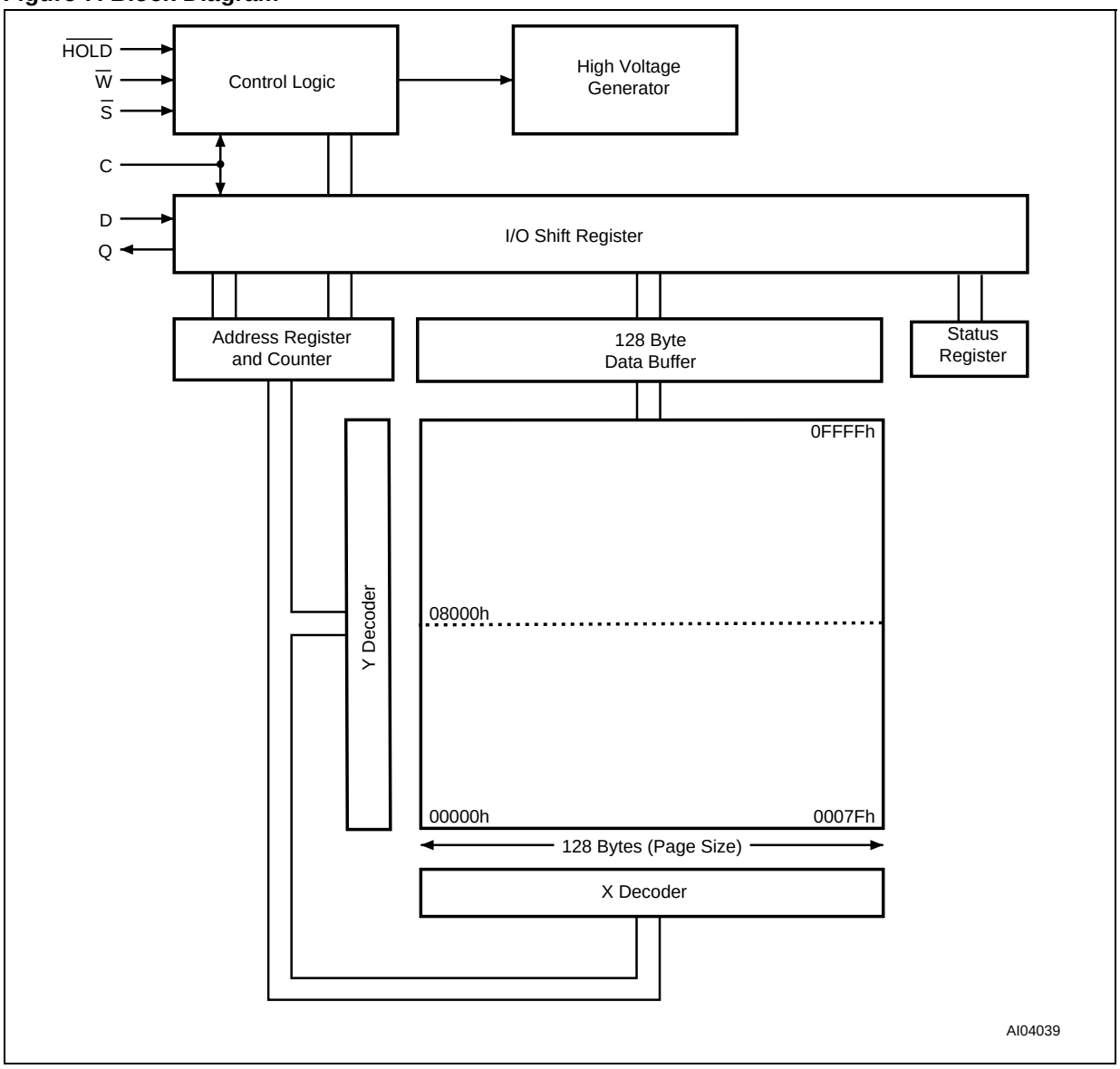
- 65536 bytes (8 bits each)
- 2 sectors (256 Kbits, 32768 bytes each)
- 512 pages (128 bytes each).

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector or Bulk Erasable (bits are erased from 0 to 1) but not Page Erasable.

Table 3. Memory Organization

Sector	Address Range	
1	08000h	0FFFFh
0	00000h	07FFFh

Figure 7. Block Diagram



INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in Table 4.

Depending on the instruction, the one-byte instruction code is followed by address bytes, or by data bytes, or by both or none. Chip Select ($\overline{S}$) must be driven High after the last bit of the instruction sequence has been shifted in.

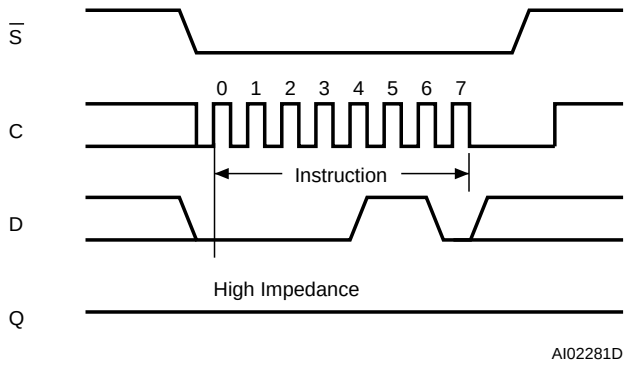
At the end of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE) or Write Status Register (WRSR) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4. Instruction Set

Instruction	Description	One-byte Instruction Code
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data Bytes	0000 0011
PP	Page Program	0000 0010
SE	Sector Erase	1101 1000
BE	Bulk Erase	1100 0111
DP	Deep Power-down	1011 1001
RES	Release from Deep Power-down, and Read Electronic Signature	1010 1011

Figure 8. Write Enable (WREN) Sequence



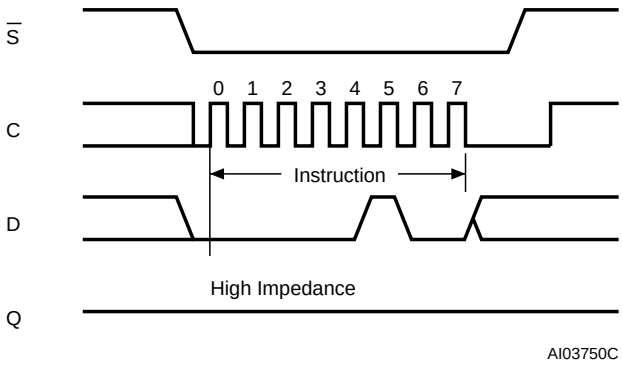
Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 8) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 9. Write Disable (WRDI) Sequence



Write Disable (WRDI)

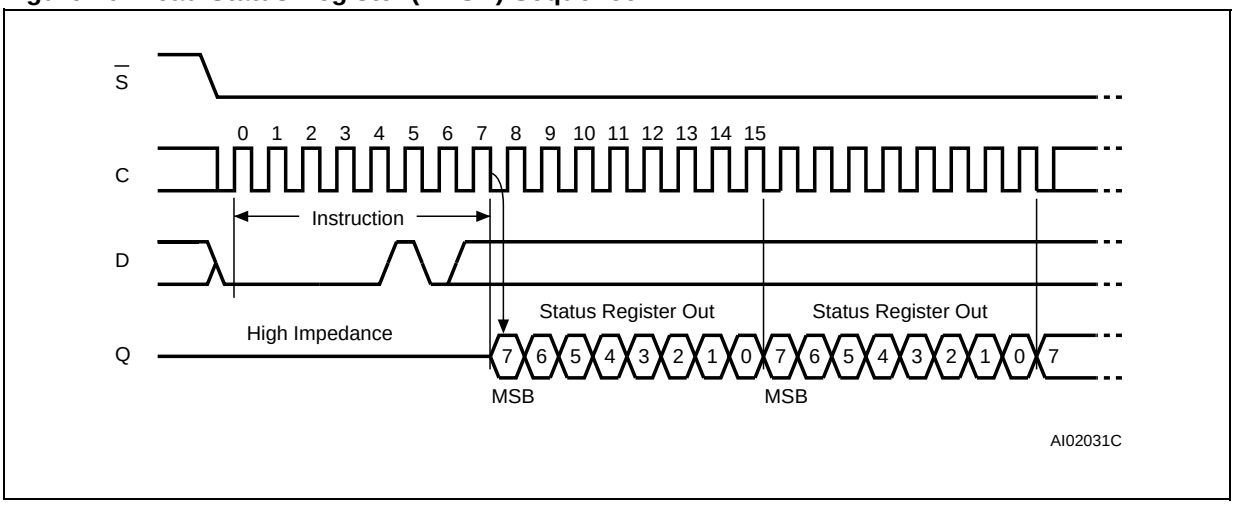
The Write Disable (WRDI) instruction (Figure 9) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

Figure 10. Read Status Register (RDSR) Sequence



Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 10.

Table 5. Status Register Format

b7							b0
SRWD	0	0	0	BP1	BP0	WEL	WIP

Note: 1. SRWD, BP1 and BP0 are non-volatile read and write bits.
2. WEL and WIP are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).

The status and control bits of the Status Register are as follows:

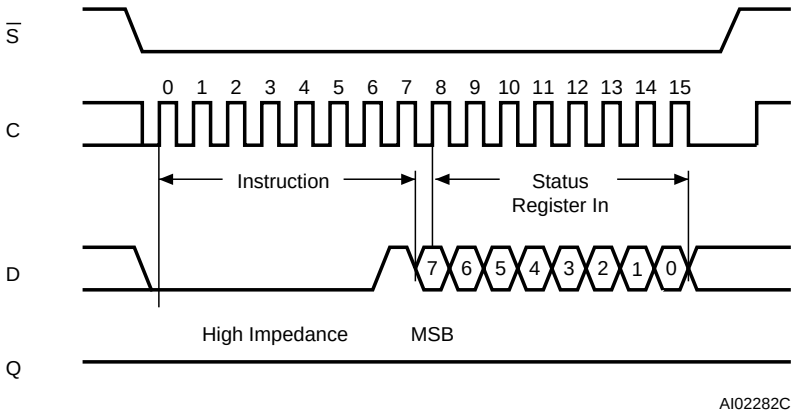
WIP bit. The Write In Process (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP1, BP0 bits. The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When both of the Block Protect (BP1, BP0) bits are set to 1, the whole memory is protected against Page Program (PP) and Sector Erase (SE) instructions. The Bulk Erase (BE) instruction is executed if, and only if, both Block Protect (BP1, BP0) bits are 0. This is summarized in Table 2. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

SRWD bit. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Figure 11. Write Status Register (WRSR) Sequence



Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on Serial Data Input (D).

The instruction sequence is shown in Figure 11.

The Write Status Register (WRSR) instruction has no effect on b6, b5, b4, b1 and b0 of the Status Register. b6, b5 and b4 are always read as 0.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 2. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SR$\overline{W}$D) bit in accordance with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

Table 6. Protection Modes

$\overline{W}$ Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory Content	
				Protected Area[1]	Unprotected Area[1]
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Protected against Page Program and Sector Erase	Ready to accept Page Program and Sector Erase instructions
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Protected against Page Program and Sector Erase	Ready to accept Page Program and Sector Erase instructions

Note: 1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in Table 2.

The protection features of the device are summarized in Table 6.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

– If Write Protect ($\overline{W}$) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.

– If Write Protect ($\overline{W}$) is driven Low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

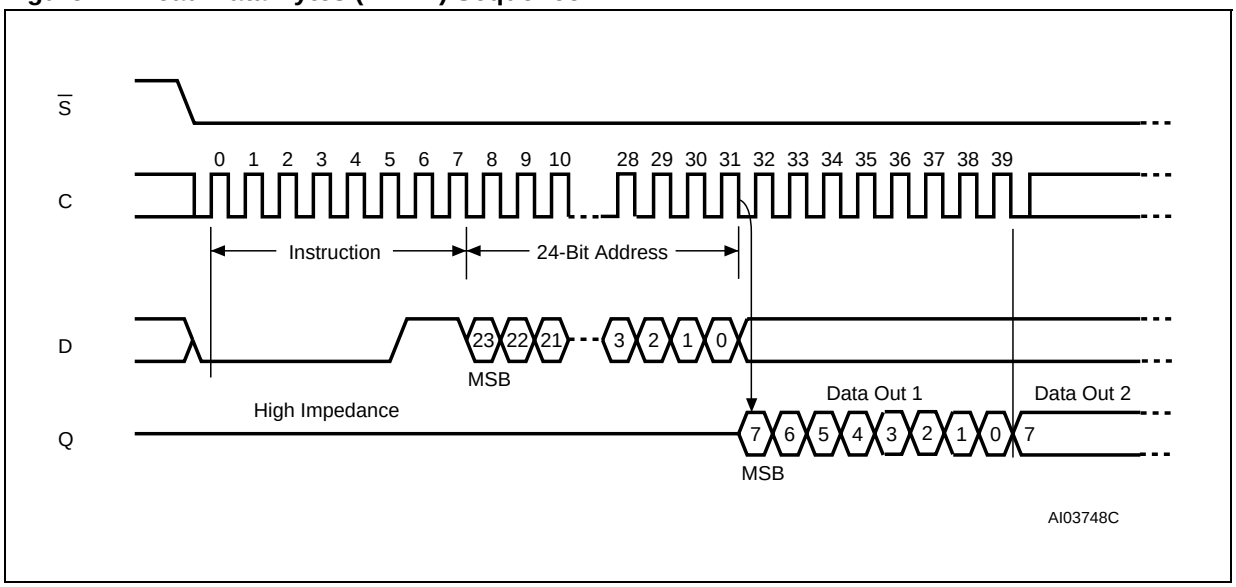
– by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low

– or by driving Write Protect ($\overline{W}$) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

If Write Protect ($\overline{W}$) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP1, BP0) bits of the Status Register, can be used.

Figure 12. Read Data Bytes (READ) Sequence



Note: 1. Address bits A23 to A16 must be set to 00h.

Read Data Bytes (READ)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

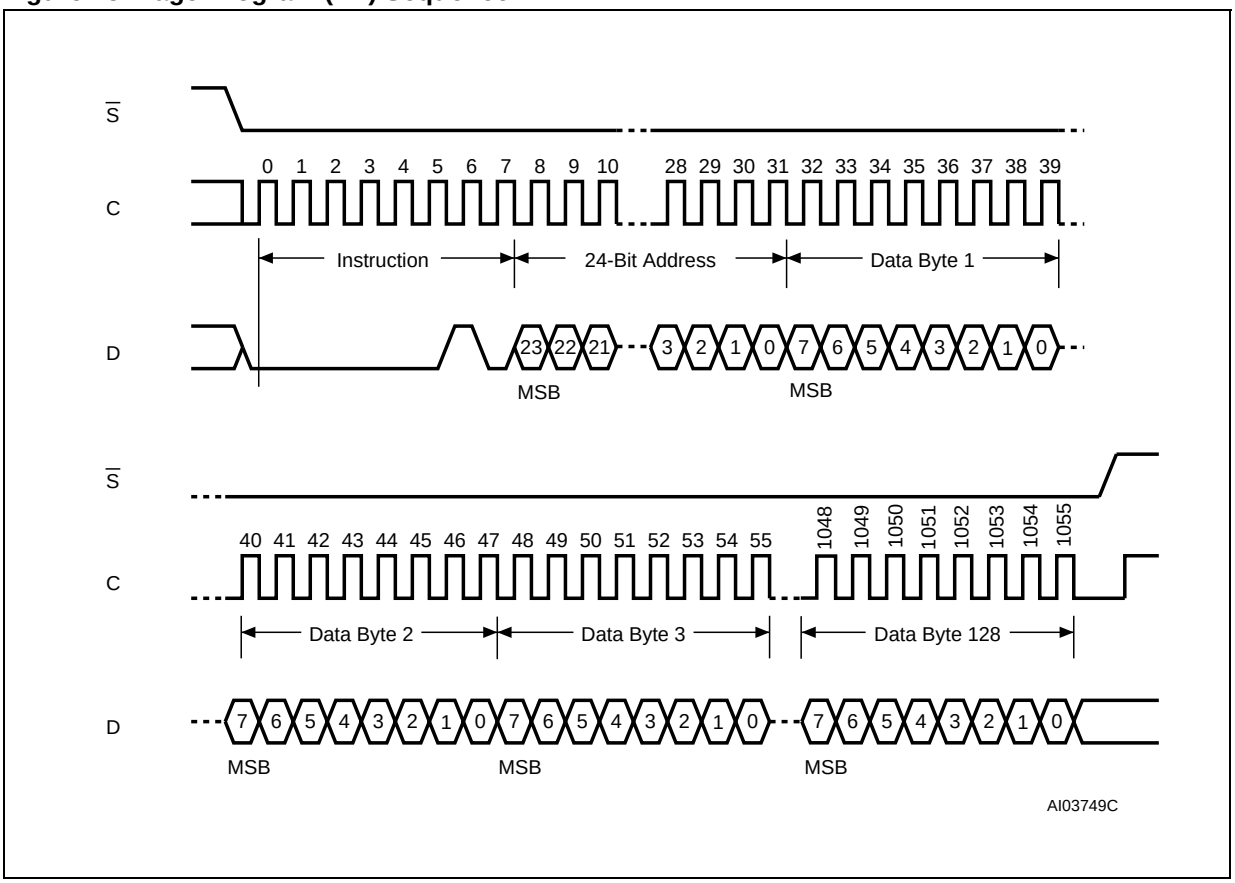
The instruction sequence is shown in Figure 12.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction.

There is no address roll-over; when the highest address (0FFFFh) is reached, the instruction should be terminated.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 13. Page Program (PP) Sequence



Note: 1. Address bits A23 to A16 must be set to 00h.

Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes (of which the most significant byte, A23-A16, must be 00h) and at least one data byte on Serial Data Input (D). If the 7 least significant address bits (A6-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are programmed from the start address of the same page (the one whose 7 least significant address bits (A6-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 13.

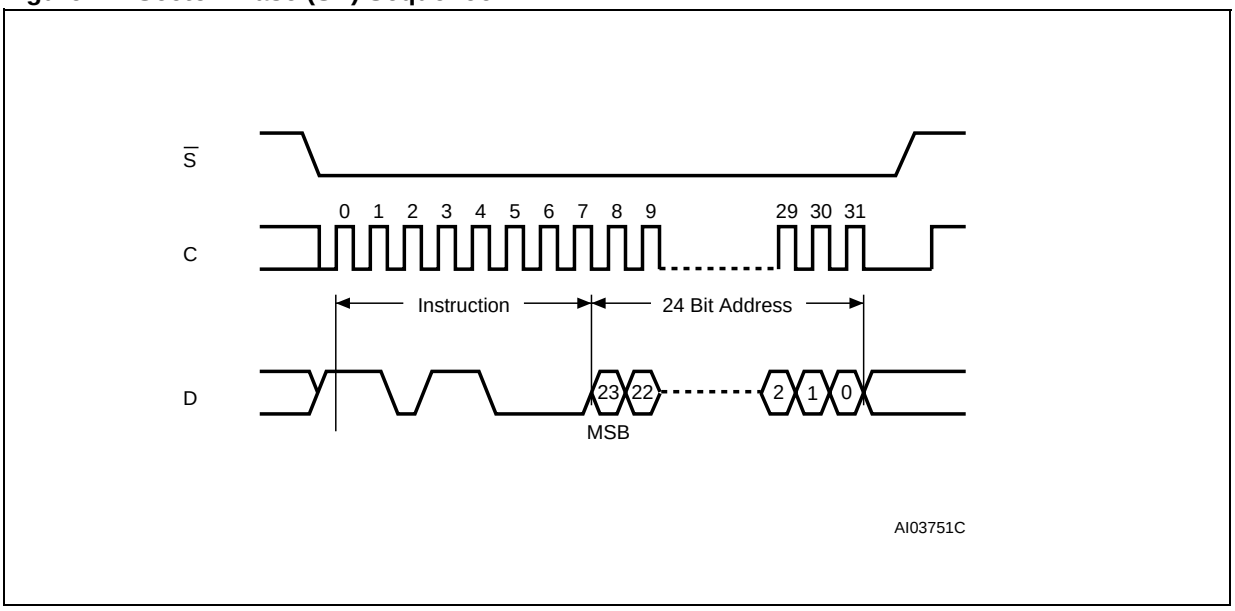
If more than 128 bytes are sent to the device, previously latched data are discarded and the last 128 data bytes are guaranteed to be programmed correctly within the same page. If less than 128 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP0, BP1) bits (see Table 2) is not executed.

Figure 14. Sector Erase (SE) Sequence



Note: 1. Address bits A23 to A16 must be set to 00h.

Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

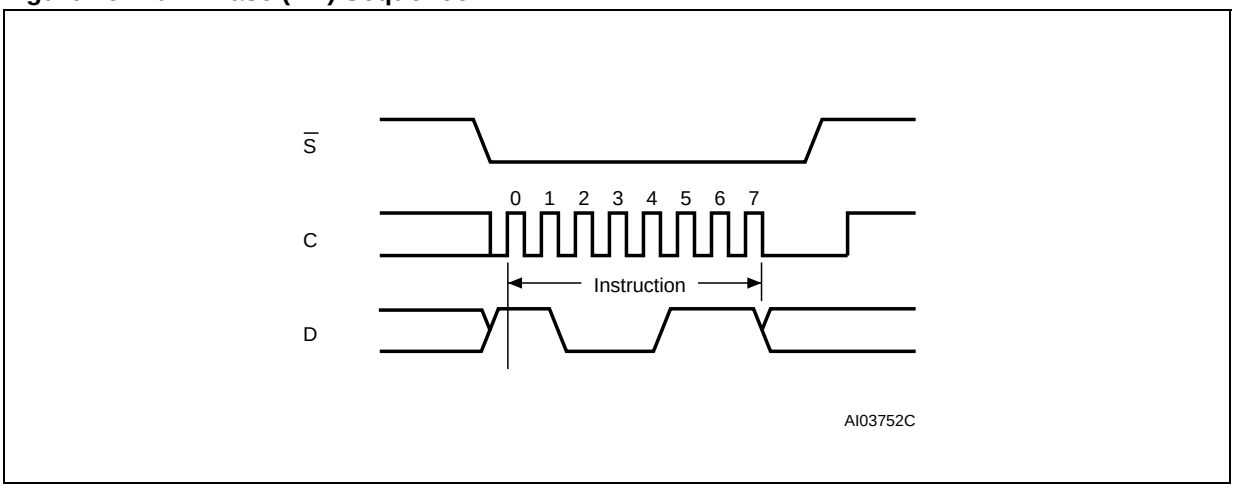
The Sector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on Serial Data Input (D). Any address inside the Sector (see Table 3) is a valid address for the Sector Erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (BP1, BP0) bits (see Table 2) is not executed.

Figure 15. Bulk Erase (BE) Sequence



Bulk Erase (BE)

The Bulk Erase (BE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

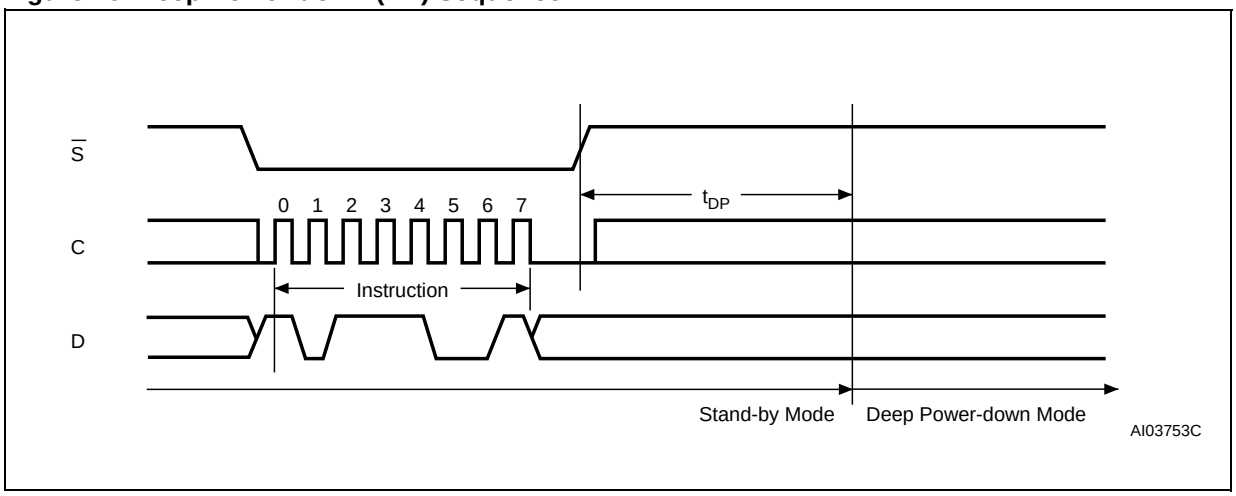
The Bulk Erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Bulk Erase (BE) instruction is executed only if both Block Protect (BP1, BP0) bits are 0. The Bulk Erase (BE) instruction is ignored if one, or more, sectors are protected.

Figure 16. Deep Power-down (DP) Sequence



Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in Table 13).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (Q).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

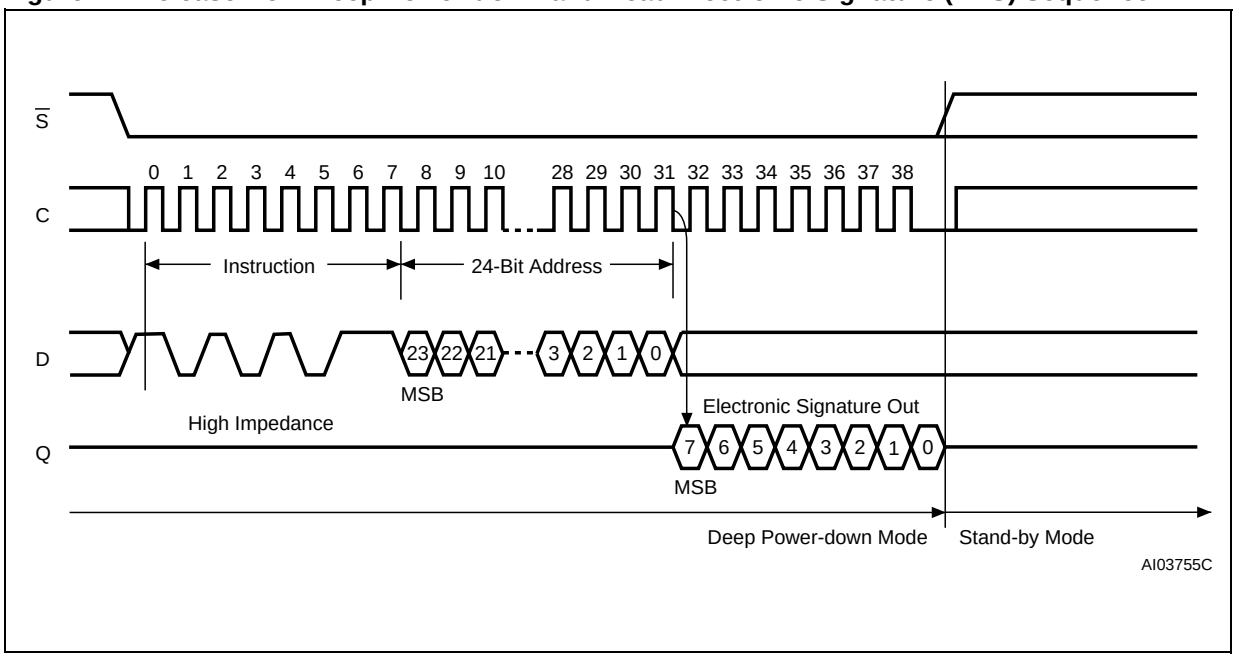
The Deep Power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 17. Release from Deep Power-down and Read Electronic Signature (RES) Sequence



Release from Deep Power-down and Read Electronic Signature (RES)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. Executing this instruction takes the device out of the Deep Power-down mode. The instruction can also be used to read, on Serial Data Output (Q), the 8-bit Electronic Signature of the device.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Electronic Signature (RES) instruction always provides access to the Electronic Signature of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Electronic Signature (RES) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

This instruction serves a second purpose. The device features an 8-bit Electronic Signature, whose value for the M25P05 is 10h. This can be read using the Release from Deep Power-down and Read Electronic Signature (RES) instruction.

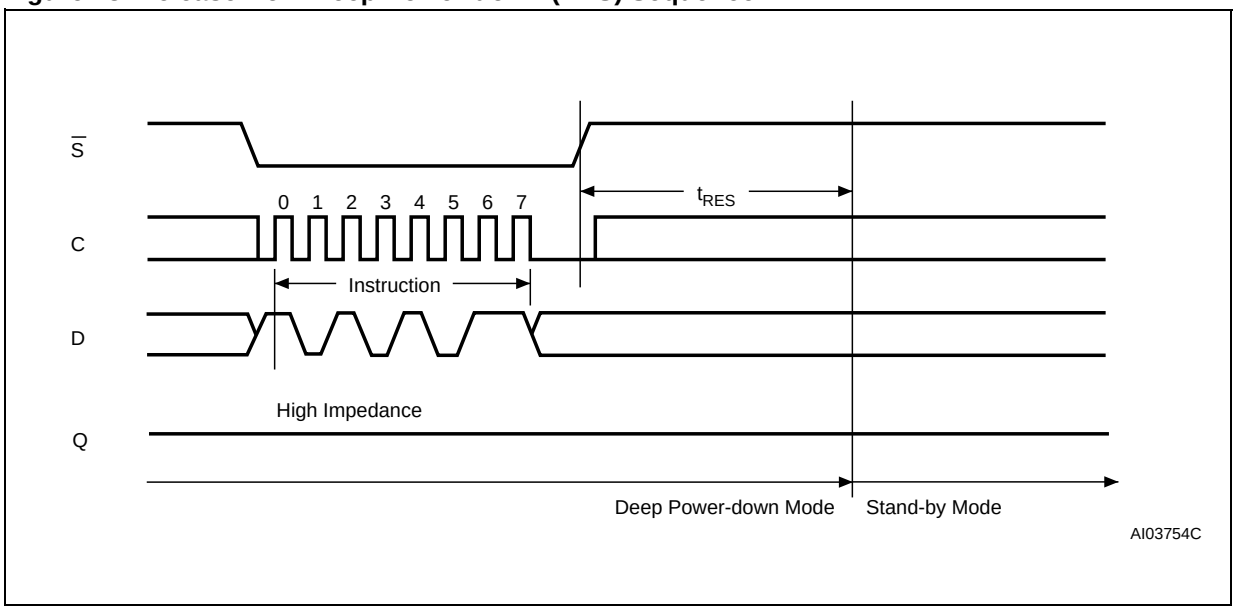
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code is followed by a dummy 3-byte address (A23-A0), each bit being latched-in on Serial Data Input (D) during the rising edge of Serial Clock (C). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 17.

The Release from Deep Power-down and Read Electronic Signature (RES) instruction is terminated by driving Chip Select ($\overline{S}$) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the Electronic Signature to be output repeatedly.

Once Chip Select ($\overline{S}$) is driven High, the device is put in the Standby mode. The device waits to be selected, so that it can receive, decode and execute instructions.

Figure 18. Release from Deep Power-down (RES) Sequence



Driving Chip Select ($\overline{S}$) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time (as shown in Figure 18), still insures that the device is taken out of the Deep Power-down mode, but incurs a delay (t_{RES}) before the device is put in Standby mode. Chip Select ($\overline{S}$) must remain High for at least t_{RES}(max), as specified in Table 14.

POWER-UP, POWER-DOWN AND DELIVERY STATE

Power-up

At Power-up, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage supplied on V_{CC}) until the supply voltage reaches V_{CC}(min), and a further t_{VSL} delay has elapsed.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device will not respond to any instruction. Similarly, when V_{CC} drops from the operating voltage, to below the POR threshold value, V_{WI}, all operations are disabled and the device will not respond to any instruction.

No instructions (including Read, Write Status Register, Program or Erase instructions) should be sent to the device until a time delay of t_{VSL} after V_{CC} has risen above the V_{CC}(min) level.

Moreover, the device ignores all Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

– t_{PUW} after V_{CC} passed the V_{WI} threshold

– t_{VSL} afterV_{CC} passed the V_{CC}(min) level

These values are specified in Table 7.

At Power-up, the device is in the following state:

– The device is in the Standby mode (not the Deep Power-down mode).

– The Write Enable Latch (WEL) bit is reset.

Figure 19. Power-up Timing

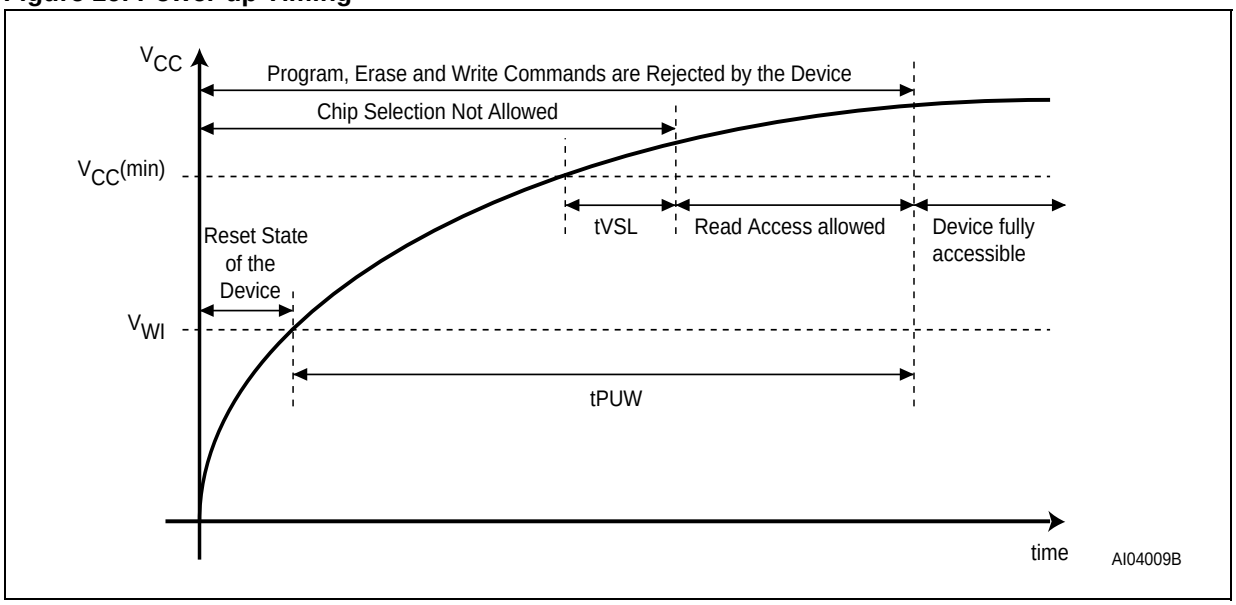


Table 7. Power-Up Timing and V_{WI} Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}[1]	V_{CC}(min) to $\overline{S}$ low	10		µs
t_{PUW}[1]	Time delay to Write instruction		15	ms
V_{WI}[1]	Write Inhibit Voltage	1.5	2.5	V

Note: 1. These parameters are characterized only.

Power-down

At Power-up and Power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

– V_{CC}(min) at Power-up

– V_{SS} at Power-down

A simple pull-up resistor on Chip Select ($\overline{S}$) can be used to insure safe and proper Power-up and Power-down.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Table 8. Initial Status Register Format

b7							b0
0	0	0	0	0	0	0	0

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering (20 seconds max.)[1]		235	°C
V_{IO}	Input and Output Voltage (with respect to Ground)	–0.6	4.0	V
V_{CC}	Supply Voltage	–0.6	4.0	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	–2000	2000	V

Note: 1. IPC/JEDEC J-STD-020A
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 10. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 11. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

Note: 1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 20. AC Measurement I/O Waveform

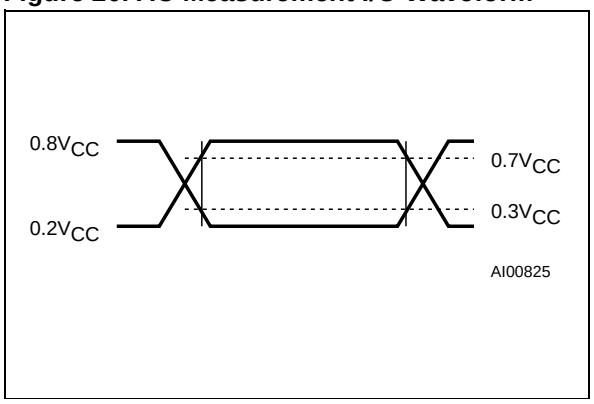


Table 12. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 20 MHz.

Table 13. DC Characteristics

Symbol	Parameter	Test Condition (in addition to those in Table 10)	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
I_{CC2}	Deep Power-down Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		5	µA
I_{CC3}	Operating Current (READ)	C = 0.1V_{CC} / 0.9.V_{CC} at 20 MHz, Q = open		3	mA
I_{CC4}	Operating Current (PP)	$\overline{S}$ = V_{CC}		15	mA
I_{CC5}	Operating Current (WRSR)	$\overline{S}$ = V_{CC}		15	mA
I_{CC6}	Operating Current (SE)	$\overline{S}$ = V_{CC}		15	mA
I_{CC7}	Operating Current (BE)	$\overline{S}$ = V_{CC}		15	mA
V_{IL}	Input Low Voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{CC}–0.2		V

Table 14. AC Characteristics

Test conditions specified in Table 10 and Table 11					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_C	Clock Frequency	D.C.	20	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time (relative to C)	10		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time (relative to C)	10		ns
t_{CH} [1]	t_{CLH}	Clock High Time	22		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	22		ns
t_{DVCH}	t_{DSU}	Data In Setup Time	5		ns
t_{CHDX}	t_{DH}	Data In Hold Time	5		ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to C)	10		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to C)	10		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	50		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		20	ns
t_{CLQV}	t_V	Clock Low to Output Valid		20	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{HLCH}		$\overline{HOLD}$ Setup Time (relative to C)	10		ns
t_{CHHH}		$\overline{HOLD}$ Hold Time (relative to C)	10		ns
t_{HHCH}		HOLD Setup Time (relative to C)	10		ns
t_{CHHL}		HOLD Hold Time (relative to C)	10		ns
t_{HHQX} [2]	t_{LZ}	HOLD to Output Low-Z		20	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ to Output High-Z		20	ns
t_{DP} [2]		$\overline{S}$ High to Deep Power-down Mode		1.6	µs
t_{RES} [2]		$\overline{S}$ High to Standby Mode		1.6	µs
t_W		Write Status Register Cycle Time		5	ms
t_{PP}		Page Program Cycle Time		5	ms
t_{SE}		Sector Erase Cycle Time		2	s
t_{BE}		Bulk Erase Cycle Time		4	s

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$
2. Value guaranteed by characterization, not 100% tested in production.

Figure 21. Serial Input Timing

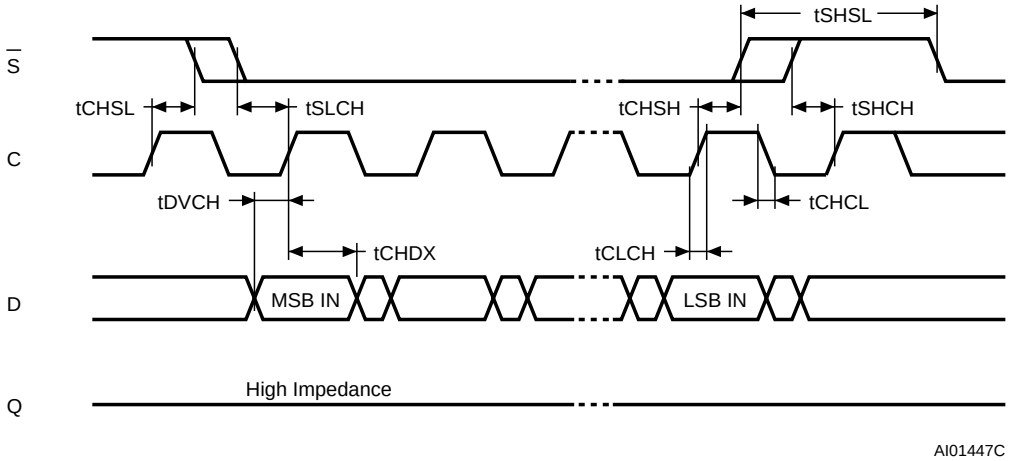


Figure 22. Hold Timing

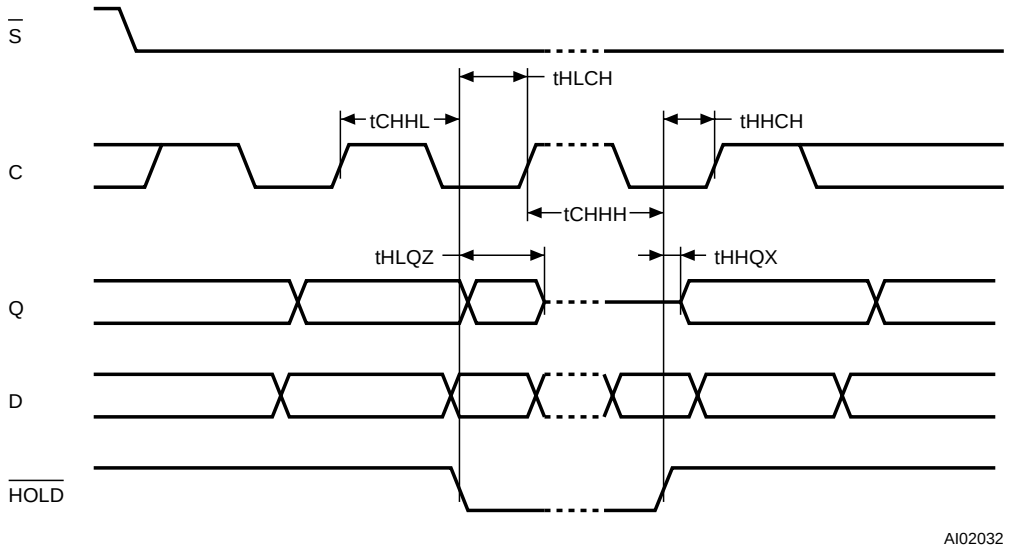
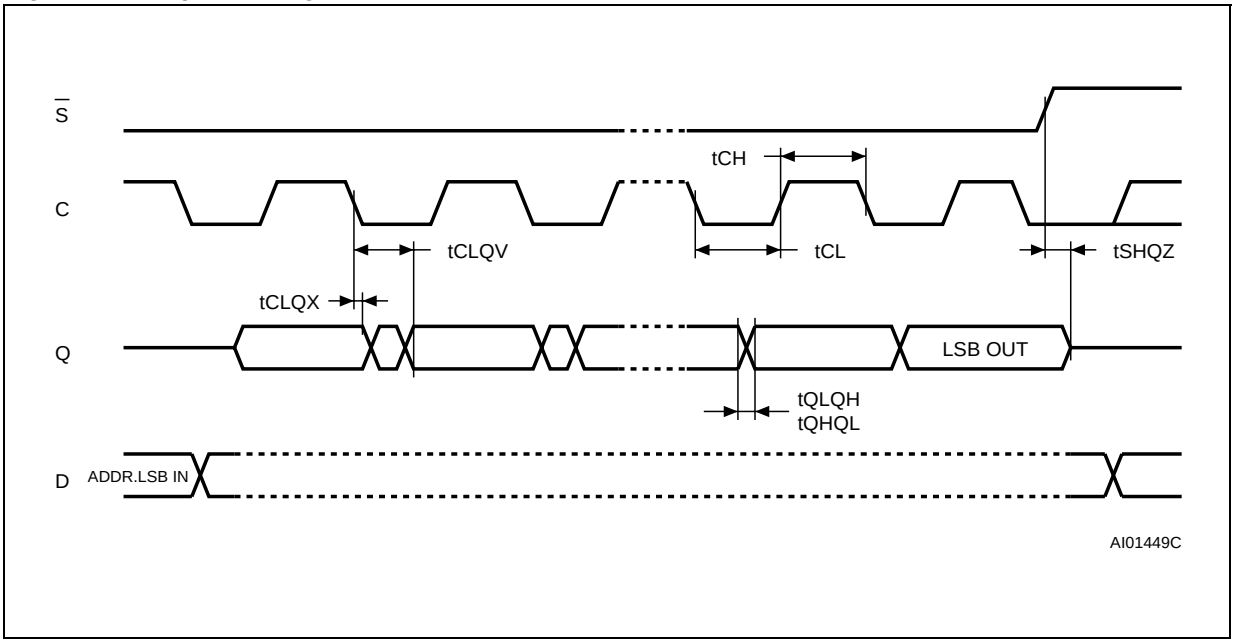
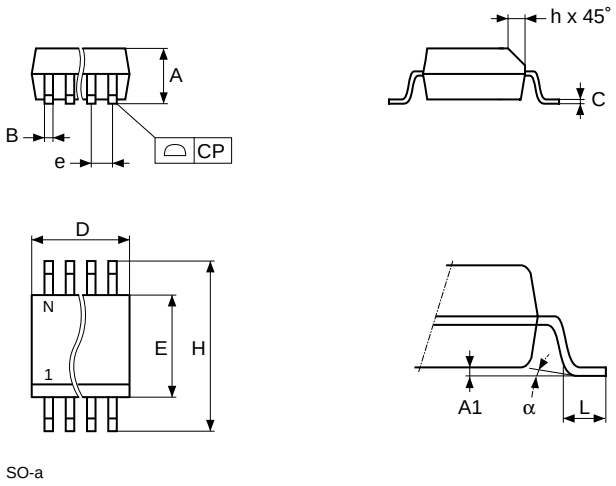


Figure 23. Output Timing



PACKAGE MECHANICAL

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width



SO-a

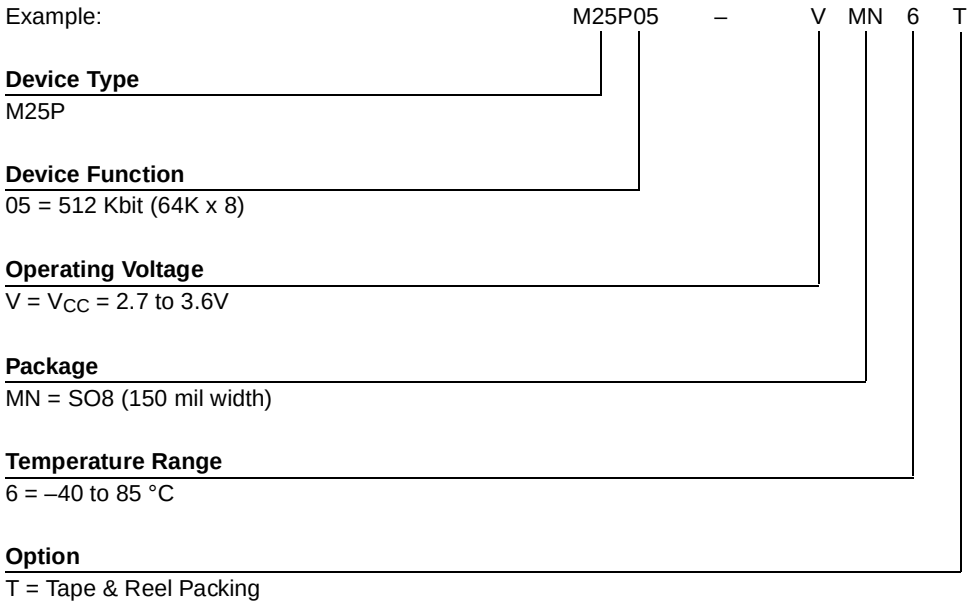
Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

PART NUMBERING

Table 15. Ordering Information Scheme



For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 16. Document Revision History

Date		Description of Revision
09-Feb-2001	1.0	Document written
26-Mar-2001	1.1	Correction to descriptions on Hold condition and Power up: no parameters changed
12-Apr-2001	1.2	Descriptions of Page Programming made more precise
25-May-2001	1.3	Serial Paged Flash Memory renamed as Serial Flash Memory
11-Sep-2001	1.4	Changes to text: Signal Description/Chip Select; Hold Condition/1st para; Protection modes; Release from Power-down and Read Electronic Signature (RES); Power-up Repositioning of several tables and illustrations without changing their contents Power-up timing illustration; SO8W package removed Changes to tables: Abs Max Ratings/V_{IO}; DC Characteristics/V_{IL}
25-Feb-2002	1.5	Product is “Not for New Design”