

Document Title**128K x8 bit 5.0V Low Power CMOS slow SRAM**Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
10	Initial Revision History Insert	Jul.14.2000	Final
11	Marking Information Add Revised <ul style="list-style-type: none"><li>- E.T (-25~85°C), I.T (-40~85°C) Part Insert</li><li>- AC Test Condition Add : 5pF Test Load</li></ul>	Dec.04.2000	Final
12	Changed Logo <ul style="list-style-type: none"><li>- HYUNDAI -&gt; hynix</li><li>- Marking Information Change</li></ul>	Apr.30.2001	Final

## DESCRIPTION

The HY628100B is a high speed, low power and 1M bit CMOS Static Random Access Memory organized as 131,072 words by 8bit. The HY628100B uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

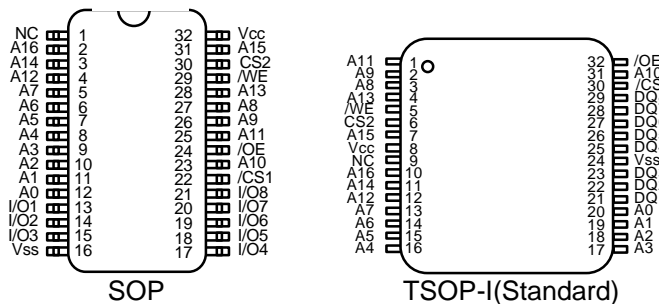
## FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(L/LL-part)
  - . 2.0V(min) data retention
- Standard pin configuration
  - . 32pin SOP - 525mil
  - . 32pin TSOP-I - 8X20(Standard)

Product No	Voltage (V)	Speed (ns)	Operation Current/I <sub>cc</sub> (mA)	Standby Current(uA)		Temperature (°C)
				L	LL	
HY628100B	4.5~5.5	50*/55/70/85	10	100	20	0~70
HY628100B-E	4.5~5.5	50*/55/70/85	10	100	30	-25~85
HY628100B-I	4.5~5.5	50*/55/70/85	10	100	30	-40~85

Comment : 50ns is available with 30pF test load.

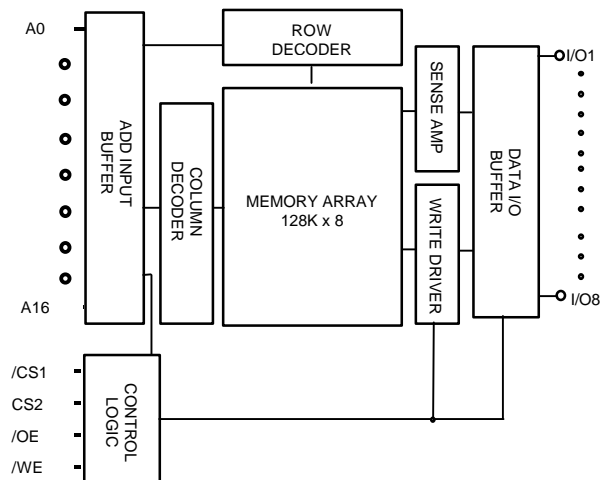
## PIN CONNECTION



## PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A16	Address Inputs
I/O1 ~ I/O8	Data Inputs / Outputs
V <sub>cc</sub>	Power(4.5V~5.5V)
V <sub>ss</sub>	Ground

## BLOCK DIAGRAM



**ORDERING INFORMATION**

Part No.	Speed	Power	Temp	Package
HY628100BLG	55/70/85	L-part	0~70°C	SOP
HY628100BLLG	55/70/85	LL-part	0~70°C	SOP
HY628100BLG-E	55/70/85	L-part	-25~85°C	SOP
HY628100BLLG-E	55/70/85	LL-part	-25~85°C	SOP
HY628100BLG-I	55/70/85	L-part	-40~85°C	SOP
HY628100BLLG-I	55/70/85	LL-part	-40~85°C	SOP
HY628100BLT1	55/70/85	L-part	0~70°C	TSOP-I(Standard)
HY628100BLLT1	55/70/85	LL-part	0~70°C	TSOP-I(Standard)
HY628100BLT1-E	55/70/85	L-part	-25~70°C	TSOP-I(Standard)
HY628100BLLT1-E	55/70/85	LL-part	-25~70°C	TSOP-I(Standard)
HY628100BLT1-I	55/70/85	L-part	-40~70°C	TSOP-I(Standard)
HY628100BLLT1-I	55/70/85	LL-part	-40~70°C	TSOP-I(Standard)

Comment : 50ns is available with 30pF test load.

**ABSOLUTE MAXIMUM RATING (1)**

Symbol	Parameter	Rating	Unit	Remark
V <sub>CC</sub> , V <sub>IN</sub> , V <sub>OUT</sub>	Power Supply, Input/Output Voltage	-0.5 to 7.0	V	
T <sub>A</sub>	Operating Temperature	0 to 70	°C	HY628100B
		-25 to 85	°C	HY628100B-E
		-40 to 85	°C	HY628100B-I
T <sub>STG</sub>	Storage Temperature	-65 to 125	°C	
P <sub>d</sub>	Power Dissipation	1.0	W	
I <sub>OUT</sub>	Data Output Current	50	mA	
T <sub>SOLDER</sub>	Lead Soldering Temperature & Time	260 • 10	°C•sec	

**Note**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**TRUTH TABLE**

/CS1	CS2	/WE	/OE	Mode	I/O	Power
H	X	X	X	Deselected	High-Z	Standby
X	L	X	X	Deselected	High-Z	Standby
L	H	H	H	Output Disabled	High-Z	Active
L	H	H	L	Read	Data Out	Active
L	H	L	X	Write	Data In	Active

**Note :**

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=don't care( V<sub>IH</sub> or V<sub>IL</sub> )

## RECOMMENDED DC OPERATING CONDITION

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  /  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  (E) /  $-40$ ;  $\bar{\text{H}}$  to  $85$ ;  $\bar{\text{H}}$ , unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
Vss	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>cc</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5(1)	-	0.8	V

Note :

1. V<sub>IL</sub> = -1.5V for pulse width less than 30ns and not 100% tested

## DC ELECTRICAL CHARACTERISTICS

V<sub>cc</sub> = 4.5V~5.5V,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  /  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  (E) /  $-40$ ;  $\bar{\text{H}}$  to  $85$ ;  $\bar{\text{H}}$ , unless otherwise specified

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit	
I <sub>LI</sub>	Input Leakage Current		$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	1	uA	
I <sub>LO</sub>	Output Leakage Current		$V_{SS} \leq V_{OUT} \leq V_{CC}$ , /CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-1	-	1	uA	
I <sub>CC</sub>	Operating Power Supply Current		/CS1 = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	-	10	mA	
I <sub>CC1</sub>	Average Operating Current		/CS1 = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> Cycle Time = Min, 100% duty, I <sub>I/O</sub> = 0mA	-	-	50	mA	
I <sub>SB</sub>	TTL Standby Current (TTL Input)		/CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	-	2	mA	
I <sub>SB1</sub>	Standby Current (CMOS Input)	HY628100B	/CS1 $\geq$ V <sub>cc</sub> - 0.2V or CS2 $\leq$ 0.2V ,	L	-	2	100	uA
				LL	-	1	20	uA
		HY628100B-E/I	V <sub>IN</sub> $\geq$ V <sub>cc</sub> - 0.2V or V <sub>IN</sub> $\leq$ V <sub>ss</sub> + 0.2V	L	-	2	100	uA
				LL	-	1	30	uA
V <sub>OL</sub>	Output Low Voltage		I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
V <sub>OH</sub>	Output High Voltage		I <sub>OH</sub> = -1mA	2.4	-	-	V	

Note : Typical values are at V<sub>cc</sub> = 5.0V, T<sub>A</sub> = 25°C

## CAPACITANCE

Temp = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I/O</sub> = 0V	8	pF

Note : These parameters are sampled and not 100% tested

### AC CHARACTERISTICS

V<sub>CC</sub> = 4.5V~5.5V, T<sub>A</sub> = 0°C to 70°C / -25°C to 85°C (E) / -40j to 85j (H), unless otherwise specified

#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
1	t <sub>RC</sub>	Read Cycle Time	55	-	70	-	85	-	ns
2	t <sub>AA*</sub>	Address Access Time	-	55	-	70	-	85	ns
3	t <sub>ACS*</sub>	Chip Select Access Time	-	55	-	70	-	85	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	25	-	35	-	45	ns
5	t <sub>CLZ</sub>	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	t <sub>CHZ</sub>	Chip Deselection to Output in High Z	0	20	0	25	0	30	ns
8	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	t <sub>OH</sub>	Output Hold from Address Change	10	-	10	-	10	-	ns
WRITE CYCLE									
10	t <sub>WC</sub>	Write Cycle Time	55	-	70	-	85	-	ns
11	t <sub>CW</sub>	Chip Selection to End of Write	45	-	60	-	70	-	ns
12	t <sub>AW</sub>	Address Valid to End of Write	45	-	60	-	70	-	ns
13	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	0	-	ns
14	t <sub>WP</sub>	Write Pulse Width	40	-	50	-	55	-	ns
15	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	ns
16	t <sub>WHZ</sub>	Write to Output in High Z	0	20	0	25	0	30	ns
17	t <sub>DW</sub>	Data to Write Time Overlap	25	-	30	-	40	-	ns
18	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	5	-	ns

Comment : t<sub>AA\*</sub> and t<sub>ACS\*</sub> can meet 50ns with 30pF test load.

### AC TEST CONDITIONS

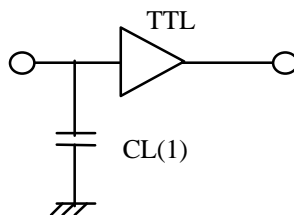
T<sub>A</sub> = 0°C to 70°C / -25°C to 85°C (E) / -40j to 85j (H), unless otherwise specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	t <sub>CLZ</sub> ,t <sub>OLZ</sub> ,t <sub>CHZ</sub> ,t <sub>OHZ</sub> ,t <sub>WHZ</sub> ,t <sub>OW</sub>	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load
		CL* = 30pF + 1TTL Load

Comment

\* : Test load is 30pF for 50ns

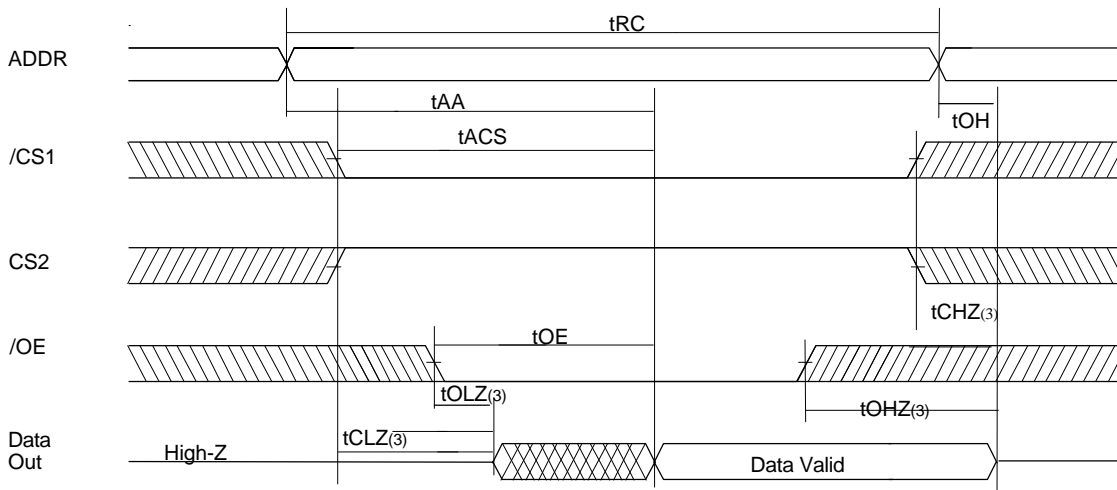
### AC TEST LOADS



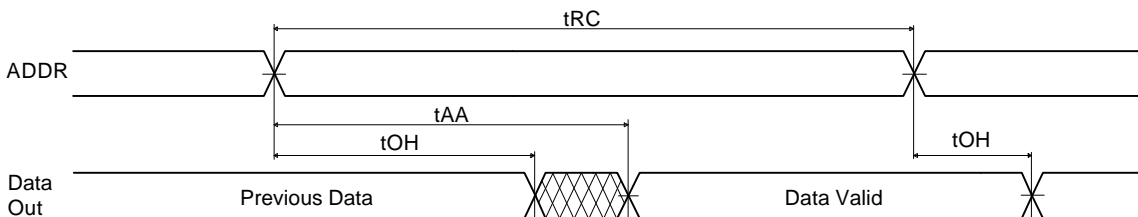
Note : Including jig and scope capacitance

**TIMING DIAGRAM**

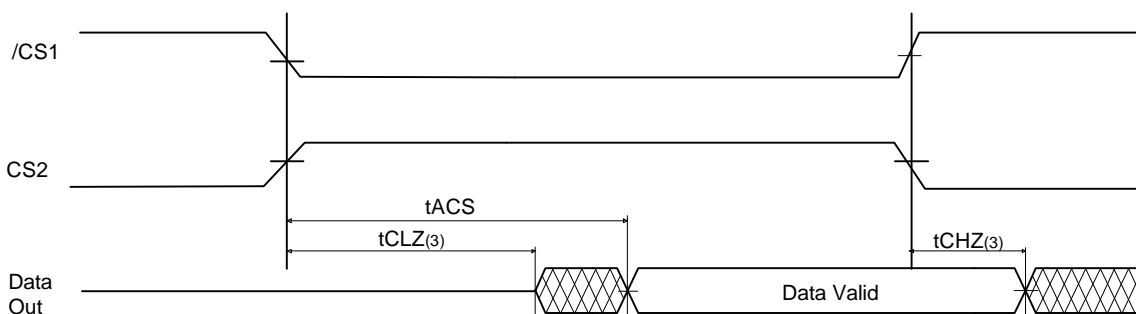
**READ CYCLE 1 (Note 1,4)**



**READ CYCLE 2 (Note 1,2,4)**



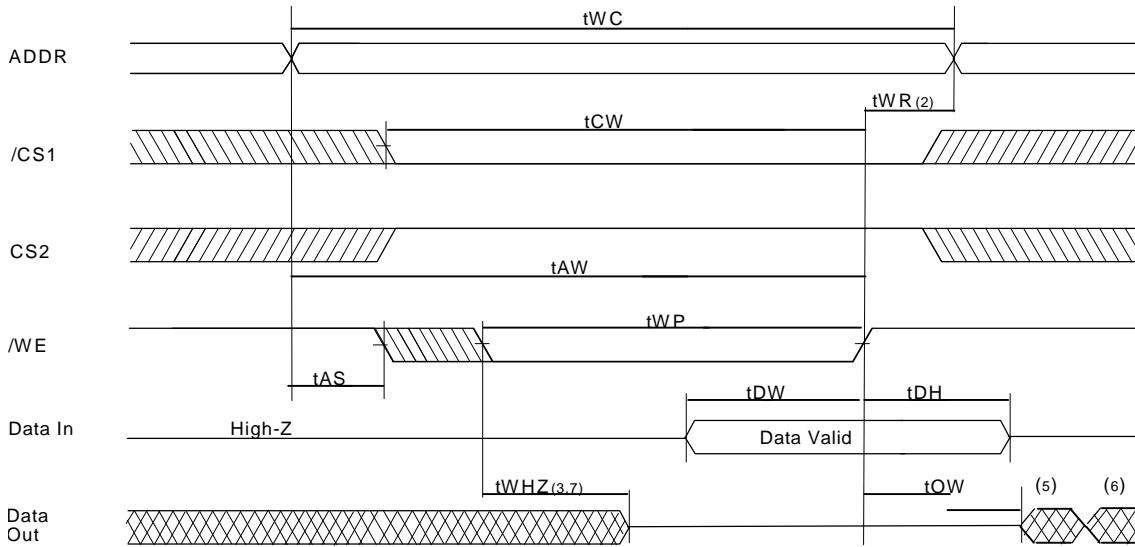
**READ CYCLE 3 (Note 1,2,4)**



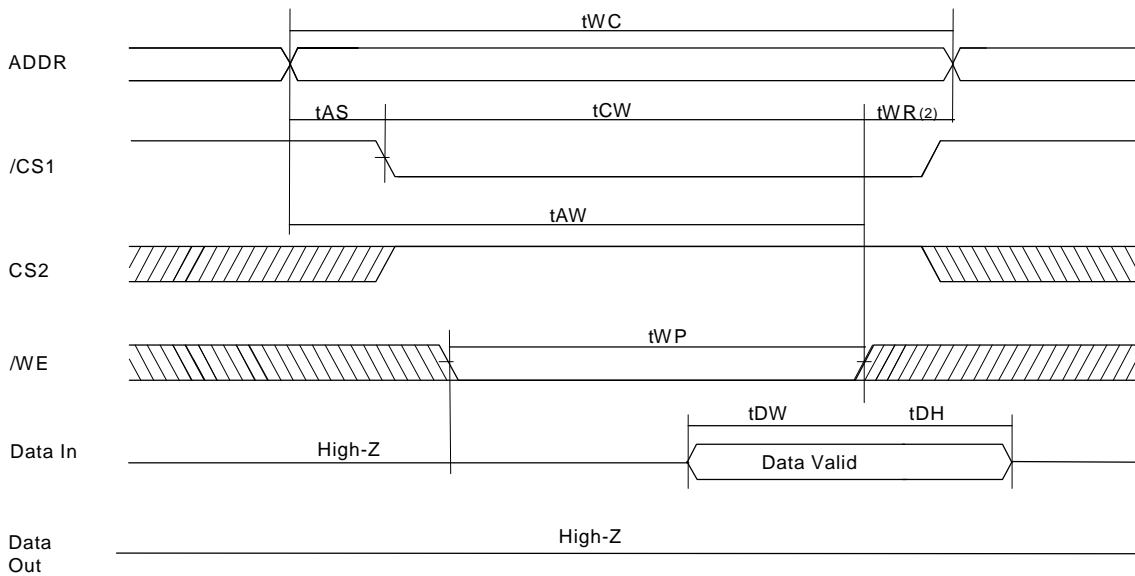
**Notes:**

1. A read occurs during the overlap of a low /OE, a high /WE, a low /CS1 and a high CS2.
2. /OE =  $V_{IL}$
3. Transition is measured  $\pm 200mV$  from steady state voltage.  
This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active  
CS2 in low for the standby, high for active

WRITE CYCLE 1(1,4,5,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,5,8) (/CS1, CS2 Controlled)



Notes:

1. A write occurs during the overlap of a low /WE, a low /CS1 and a high CS2.
2. t<sub>WR</sub> is measured from the earlier of /CS1 or /WE going high or CS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the the /CS1 low transition and CS2 high transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. Transition is measured +200mV from steady state.  
This parameter is sampled and not 100% tested.
9. /CS1 in high for the standby, low for active  
CS2 in low for the standby, high for active

**DATA RETENTION ELECTRIC CHARACTERISTIC**

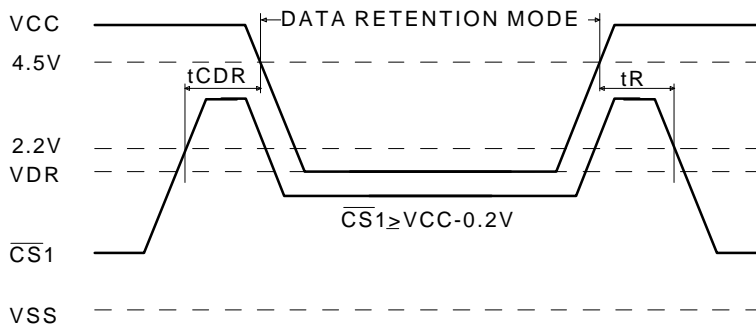
TA = 0°C to 70°C / -25°C to 85°C (E) / -40j to 85j (H), unless otherwise specified

Sym	Parameter		Test Condition	Min	Typ	Max	Unit	
VDR	Vcc for Data Retention		/CS1 ≥ Vcc - 0.2V or CS2 ≤ 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ Vss + 0.2V	2.0	-	-	V	
ICCDR	Data Retention Current	HY628100B	Vcc = 3.0V, /CS1 ≥ Vcc - 0.2V or CS2 ≤ 0.2V,	L	-	2	50	uA
				LL	-	1	10	uA
		HY628100B-E/I	VIN ≥ Vcc - 0.2V or VIN ≤ Vss + 0.2V	L	-	2	50	uA
				LL	-	1	15	uA
tCDR	Chip Deselect to Data Retention Time			0	-	-	ns	
tR	Operating Recovery Time			tRC (2)	-	-	ns	

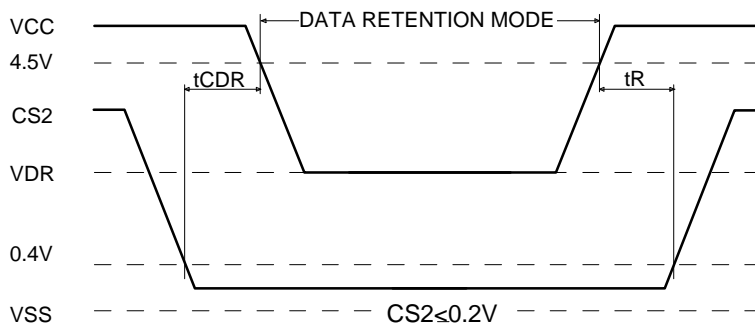
Notes:

1. Typical values are under the condition of TA = 25°C.
2. tRC is read cycle time.

**DATA RETENTION TIMING DIAGRAM 1**



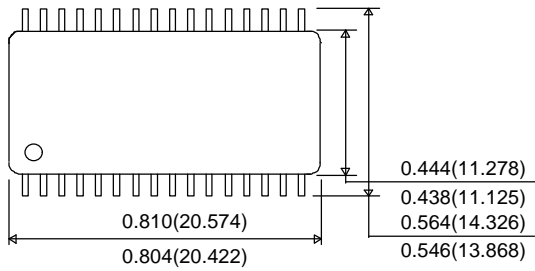
**DATA RETENTION TIMING DIAGRAM 2**



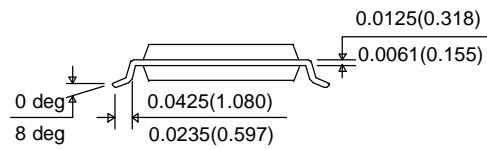
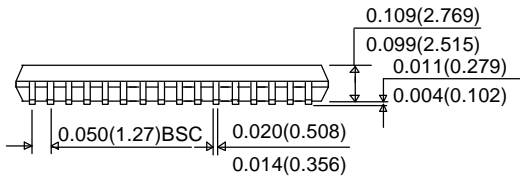


**PACKAGE INFORMATION**

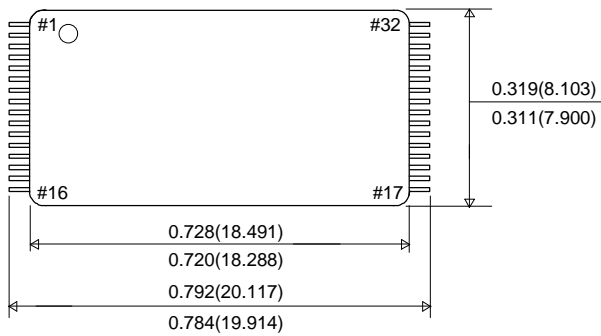
32pin 525mil Small Outline Package(G)



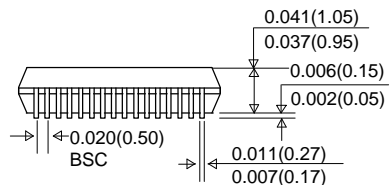
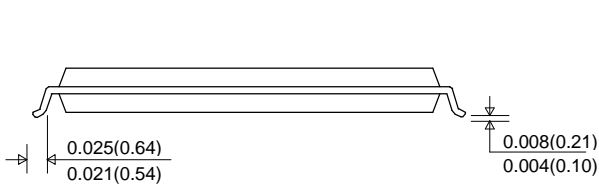
UNIT : INCH(mm)



32pin 8x20mm Thin Small Outline Package Standard(T1)



UNIT : INCH(mm)



**MARKING INFORMATION**

Package	Marking Example																																																
SOP	<table border="1"> <tr> <td>h</td><td>y</td><td>n</td><td>i</td><td>x</td><td></td><td></td><td></td><td></td><td></td><td>K</td><td>O</td><td>R</td><td>E</td><td>A</td> </tr> <tr> <td>H</td><td>Y</td><td>6</td><td>2</td><td>8</td><td>1</td><td>0</td><td>0</td><td>B</td><td></td><td></td><td></td><td></td><td></td><td></td> </tr> <tr> <td>y</td><td>y</td><td>w</td><td>w</td><td>p</td><td></td><td></td><td></td><td></td><td></td><td>c</td><td>c</td><td>G</td><td>-</td><td>s</td><td>s</td><td>t</td> </tr> </table>	h	y	n	i	x						K	O	R	E	A	H	Y	6	2	8	1	0	0	B							y	y	w	w	p						c	c	G	-	s	s	t	
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Index	
• hynix	: hynix Logo
• KOREA	: Origin Country
• HY628100B	: Part Name
• yy	: Year ( ex : 00 = year 2000, 01 = year 2001 )
• ww	: Work Week ( ex : 12 = ww12 )
• p	: Process Code
• cc	: Power Consumption
	- L : Low Power
	- LL : Low Low Power
• G / T1	: Package Type
	- G : SOP
	- T1 : TSOP-I
• ss	: Speed
	- 55 : 55ns
	- 70 : 70ns
• t	: Temperature
	- Blank : Commercial ( 0 ~ 70 °C )
	- E : Extended ( -25 ~ 85 °C )
	- I : Industrial ( -40 ~ 85 °C )
<b>Note</b>	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item (Except hynix)

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