# Twelve Output Differential Buffer for PCIe Gen 1 and Gen 2

# ICS9DB1200B

# Description

DB1200 Intel Yellow Cover Device. The **ICS9DB1200** is an Intel DB1200 Differential Buffer Specification device. This buffer provides 12 differential clocks at frequencies ranging from 100MHz to 400 MHz. The **ICS9DB1200** is driven by a differential output from a CK409B/CK410B/CK505 main clock generator.

### Features/Benefits

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread
- Supports undriven differential outputs in Power Down Mode for power management.

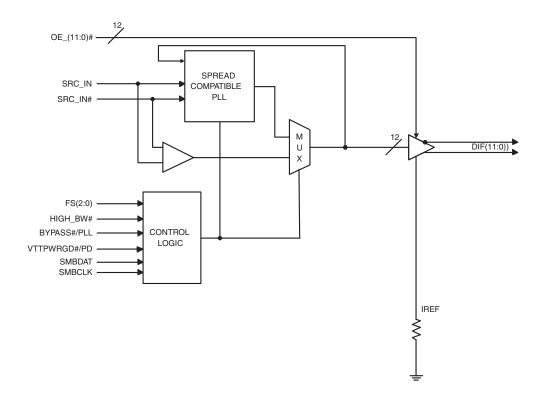
# **Output Features**

- 12 0.7V current-mode differential output pairs.
- Supports zero delay buffer mode and fanout mode.
- Bandwidth programming available.
- 100-400.MHz operation in PLL mode
- 33-400 MHz operation in Bypass mode

### **Key Specifications**

- Output cycle-cycle jitter < 50ps.
- Output to output skew: 50ps
- Phase jitter: PCIe Gen2 < 3.1ps rms
- 64-pin TSSOP Package
- Available in RoHS compliant packaging

# **Funtional Block Diagram**



# **Pin Configuration**

VDD DIF_IN# GND OE0# DIF_0 DIF_0 UDF_0 UDF_0 UDF_0 UDF_0 UDF_0 UDF_1 DIF_1 DIF_1 DIF_1 DIF_2 DIF_2 DIF_2 DIF_2 DIF_2 UDF_3 DIF_3 DIF_3 DIF_3 DIF_3 DIF_4 DIF_4 UDF_4 UDF_4 UDF_5 DIF_5 DIF_5 N/C HIGH_BW# FS2 SMBCLK	$\begin{array}{c} 2\\ 3\\ 4\\ 5\\ 6\\ 7\\ 8\\ 9\\ 10\\ 11\\ 12\\ 13\\ 14\\ 15\\ 16\\ 17\\ 18\\ 20\\ 22\\ 23\\ 24\\ 5\\ 26\\ 27\\ 28\\ 9\\ 30\\ 31\\ \end{array}$	6 6 6 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	<ul> <li>VDDA</li> <li>AGND</li> <li>IREF</li> <li>FSO</li> <li>OE11#</li> <li>DIF_11</li> <li>DIF_11</li> <li>DIF_11#</li> <li>VDD</li> <li>GND</li> <li>OE10#</li> <li>DIF_10</li> <li>DIF_10</li> <li>DIF_10#</li> <li>OE9#</li> <li>DIF_9</li> <li>GND</li> <li>VDD</li> <li>OIF_9#</li> <li>GND</li> <li>VDD</li> <li>OIF_9#</li> <li>GND</li> <li>VDD</li> <li>OIF_9#</li> <li>GND</li> <li>VD</li> <li>OIF_9#</li> <li>GND</li> <li>VD</li> <li>OIF_9#</li> <li>GND</li> <li>VD</li> <li>OIF_9#</li> <li>GND</li> <li>VDD</li> <li>OIF_9#</li> <li>GND</li> <li>VD</li> <li>OIF_9#</li> <li>GND</li> <li>VD</li> <li>OIF_9#</li> <li>GND</li> <li>VD</li> <li>OIF_6#</li> <li>VTTPWRGD#/PD</li> <li>BYPASS#/PLL</li> <li>FS1</li> <li>SMBDAT</li> </ul>
		64-TSSOP	

64-TSSOP

# **Frequency Select Table**

FS∟2 B0b2	FS∟1 B0b1	FS <sub>L</sub> 0 B0b0	Input MHz	DIF_x; MHz
0	0	0	266.66	266.66
0	0	1	133.33	133.33
0	1	0	200.00	200.00
0	1	1	166.66	166.66
1	0	0	333.33	333.33
1	0	1	100.00	100.00
1	1	0	400.00	400.00
1	1	1	Hi-Z	Hi-Z

1.  $FS_L(2:0)$  are 3.3V tolerant low-threshold inputs.

Please see VIL\_FS and VIH\_FS specifications in

the Input/Supply/Common Output Parameters Table for correct values.

**IDT™/ICS™** Twelve Output Differential Buffer for PCIe Gen 1 and Gen 2

ICS9DB1200B REV A 03/21/07

# **Pin Description**

1VDDPWRPower supply, nominal 3.3V2DIF_IN#IN0.7 V Differential TRUE input3DIF_IN#IN0.7 V Differential Complementary Input4GNDPWRGround pin.5OE0#INActive low input for enabling DIF pair 0. 1 = tristate outputs, 0 = enable outputs6DIF_0OUT0.7V differential complement clock output7DIF_0#OUT0.7V differential complement clock output8VDDPWRForund pin.9GNDPWRGround pin.10OE1#INActive low input for enabling DIF pair 1. 1 = tristate outputs, 0 = enable outputs11DIF_1OUT0.7V differential rue clock output12DIF_1#OUT0.7V differential rue clock output13OE2#INActive low input for enabling DIF pair 2. 1 = tristate outputs, 0 = enable outputs14DIF_2OUT0.7V differential rue clock output15DIF_2#OUT0.7V differential complement clock output16GNDPWRGround pin.17VDDPWRPower supply, nominal 3.3V18OE3#INActive low input for enabling DIF pair 3. 1 = tristate outputs, 0 = enable outputs20DIF_3OUT0.7V differential rue clock output21OE4#INActive low input for enabling DIF pair 3. 1 = tristate outputs, 0 = enable outputs22DIF_3OUT0.7V differential rue clock output23DIF	PIN #	PIN NAME	TYPE	DESCRIPTION	
3         DIF_IN#         IN         0.7 V Differential Complementary Input           4         GND         PWR         Ground pin.           5         OE0#         IN         Active low input for enabling DIF pair 0.           7         DIF_0#         OUT         0.7V differential complement clock output           8         VDD         PWR         Power supply, nominal 3.3V           9         GND         PWR         Power supply, nominal 3.3V           9         GND         PWR         Ground pin.           10         OE1#         IN         Active low input for enabling DIF pair 1.           11         DIF_1#         OUT         0.7V differential complement clock output           12         DIF_1#         OUT         0.7V differential true clock output           13         OE2#         IN         Active low input for enabling DIF pair 2.           14         DIF_2#         OUT         0.7V differential true clock output           15         DIF_2#         OUT         0.7V differential complement clock output           16         GND         PWR         Power supply, nominal 3.3V           18         OE3#         IN         Active low input for enabling DIF pair 3.           19         DIF_3	1		PWR	Power supply, nominal 3.3V	
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9       GND       PWR       Ground pin.         10       OE1#       IN       Active low input for enabling DIF pair 1.         11       DIF_1       OUT       0.7V differential true clock output         12       DIF_1#       OUT       0.7V differential complement clock output         13       OE2#       IN       Active low input for enabling DIF pair 2.         14       DIF_2       OUT       0.7V differential true clock output         15       DIF_2#       OUT       0.7V differential true clock output         16       GND       PWR       Ground pin.         17       VDD       PWR       Ground pin.         18       OE3#       IN       1 = tri-state outputs, 0 = enable outputs         19       DIF_3       OUT       0.7V differential true clock output         20       DIF_3#       OUT       0.7V differential complement clock output         21       OE4#       IN       1 = tri-state outputs, 0 = enable outputs         22       DIF_4       OUT       0.7V differential complement clock output         23       DIF_5       OUT       0.7V differential complement clock output         24       VDD       PWR       Power supply, nominal 3.3V         25	7				
10OE1#INActive low input for enabling DIF pair 1. 1 = tri-state outputs, 0 = enable outputs11DIF_1OUT0.7V differential true clock output12DIF_1#OUT0.7V differential complement clock output13OE2#INActive low input for enabling DIF pair 2. 1 = tri-state outputs, 0 = enable outputs14DIF_2OUT0.7V differential true clock output15DIF_2#OUT0.7V differential true clock output16GNDPWRGround pin.17VDDPWRPower supply, nominal 3.3V18OE3#INActive low input for enabling DIF pair 3. 1 = tri-state outputs.19DIF_3OUT0.7V differential true clock output20DIF_3OUT0.7V differential complement clock output21OE4#INActive low input for enabling DIF pair 3. 1 = tri-state outputs.22DIF_3#OUT0.7V differential complement clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs.22DIF_4OUT0.7V differential complement clock output23DIF_4#OUT0.7V differential true clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential complement clock output28DIF_5#O	8	VDD	PWR	Power supply, nominal 3.3V	
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11DIF_1OUT0.7V differential true clock output12DIF_1#OUT0.7V differential complement clock output13OE2#INActive low input for enabling DIF pair 2. 1 = tri-state outputs, 0 = enable outputs14DIF_2OUT0.7V differential true clock output15DIF_2#OUT0.7V differential complement clock output16GNDPWRGround pin.17VDDPWRPower supply, nominal 3.3V18OE3#INActive low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs19DIF_3OUT0.7V differential true clock output20DIF_3#OUT0.7V differential complement clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4OUT0.7V differential true clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRPower supply, nominal 3.3V26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential true clock output29N/CN/CN/C30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1= Low31FS2INFrequency select pin.<	10	OE1#	IN		
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13 $OE2#$ INActive low input for enabling DIF pair 2. 1 = tri-state outputs, 0 = enable outputs14 $DIF_2$ $OUT$ $0.7V$ differential true clock output15 $DIF_2#$ $OUT$ $0.7V$ differential complement clock output16 $GND$ $PWR$ $Ground pin.$ 17 $VDD$ $PWR$ Power supply, nominal 3.3V18 $OE3#$ $IN$ Active low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs19 $DIF_3$ $OUT$ $0.7V$ differential true clock output20 $DIF_3#$ $OUT$ $0.7V$ differential complement clock output21 $OE4#$ $IN$ Active low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22 $DIF_4$ $OUT$ $0.7V$ differential complement clock output23 $DIF_4#$ $OUT$ $0.7V$ differential complement clock output24 $VDD$ $PWR$ Power supply, nominal 3.3V25 $GND$ $PWR$ Ground pin.26 $OE5#$ $IN$ Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27 $DIF_5$ $OUT$ $0.7V$ differential complement clock output28 $DIF_5#$ $OUT$ $0.7V$ differential complement clock output29 $N/C$ $N/C$ $N/C$ No Connection.30 $HIGH_BW#$ $IN$ $3.3V$ input for selecting PLL Band Width $0 = High, 1=Low$ 31 $FS2$ $IN$ $Frequency select pin.$					
14DIF_2OUT0.7V differential true clock output15DIF_2#OUT0.7V differential complement clock output16GNDPWRGround pin.17VDDPWRPower supply, nominal 3.3V18OE3#INActive low input for enable outputs, $0 = enable outputs$ 19DIF_3OUT0.7V differential complement clock output20DIF_3#OUT0.7V differential true clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, $0 = enable outputs$ 22DIF_4OUT0.7V differential complement clock output23DIF_4#OUT0.7V differential true clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CN/C30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1= Low31FS2INFrequency select pin.	10				
15DIF_2#OUT0.7V differential complement clock output16GNDPWRGround pin.17VDDPWRPower supply, nominal 3.3V18OE3#INActive low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs19DIF_3OUT0.7V differential true clock output20DIF_3#OUT0.7V differential complement clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4#OUT0.7V differential complement clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential rue clock output28DIF_5#OUT0.7V differential rue clock output29N/CN/CN/C30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1= Low31FS2INFrequency select pin.	13	OE2#	IN	1 = tri-state outputs, 0 = enable outputs	
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17VDDPWRPower supply, nominal 3.3V18OE3#INActive low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs19DIF_3OUT0.7V differential true clock output20DIF_3#OUT0.7V differential complement clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential complement clock output23DIF_4#OUT0.7V differential complement clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CN/CNo Connection.30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1 = Low31FS2INFrequency select pin.	15	DIF_2#	OUT	0.7V differential complement clock output	
18       OE3#       IN       Active low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs         19       DIF_3       OUT       0.7V differential true clock output         20       DIF_3#       OUT       0.7V differential complement clock output         21       OE4#       IN       Active low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs         22       DIF_4       OUT       0.7V differential true clock output         23       DIF_4#       OUT       0.7V differential complement clock output         24       VDD       PWR       Power supply, nominal 3.3V         25       GND       PWR       Ground pin.         26       OE5#       IN       Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs         27       DIF_5       OUT       0.7V differential true clock output         28       DIF_5#       OUT       0.7V differential complement clock output         29       N/C       N/C       Nc       No Connection.         30       HIGH_BW#       IN       3.3V input for selecting PLL Band Width 0 = High, 1 = Low         31       FS2       IN       Frequency select pin.	16	GND	PWR	Ground pin.	
18DE3#IN1 = tri-state outputs, 0 = enable outputs19DIF_3OUT0.7V differential true clock output20DIF_3#OUT0.7V differential complement clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4#OUT0.7V differential true clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CN/CNo Connection.30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1 = Low31FS2INFrequency select pin.	17	VDD	PWR	Power supply, nominal 3.3V	
19DIF_3OUT0.7V differential true clock output20DIF_3#OUT0.7V differential true clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4#OUT0.7V differential true clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CN/C30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1 = Low31FS2INFrequency select pin.	18	OE3#	IN	Active low input for enabling DIF pair 3.	
20DIF_3#OUT0.7V differential complement clock output21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4#OUT0.7V differential complement clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CNo Connection.30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1= Low31FS2INFrequency select pin.	10				
21OE4#INActive low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4#OUT0.7V differential complement clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CNo Connection.30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1= Low31FS2INFrequency select pin.	19		OUT		
21UE4#IN1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4#OUT0.7V differential complement clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CNo Connection.30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1 = Low31FS2INFrequency select pin.	20	DIF_3#	OUT		
1 = tri-state outputs, 0 = enable outputs22DIF_4OUT0.7V differential true clock output23DIF_4#OUT0.7V differential complement clock output24VDDPWRPower supply, nominal 3.3V25GNDPWRGround pin.26OE5#INActive low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs27DIF_5OUT0.7V differential true clock output28DIF_5#OUT0.7V differential complement clock output29N/CN/CNo Connection.30HIGH_BW#IN3.3V input for selecting PLL Band Width 0 = High, 1 = Low31FS2INFrequency select pin.	21	OF4#	IN		
23       DIF_4#       OUT       0.7V differential complement clock output         24       VDD       PWR       Power supply, nominal 3.3V         25       GND       PWR       Ground pin.         26       OE5#       IN       Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs         27       DIF_5       OUT       0.7V differential true clock output         28       DIF_5#       OUT       0.7V differential complement clock output         29       N/C       N/C       No Connection.         30       HIGH_BW#       IN       3.3V input for selecting PLL Band Width 0 = High, 1= Low         31       FS2       IN       Frequency select pin.					
24       VDD       PWR       Power supply, nominal 3.3V         25       GND       PWR       Ground pin.         26       OE5#       IN       Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs         27       DIF_5       OUT       0.7V differential true clock output         28       DIF_5#       OUT       0.7V differential complement clock output         29       N/C       N/C       No Connection.         30       HIGH_BW#       IN       3.3V input for selecting PLL Band Width 0 = High, 1 = Low         31       FS2       IN       Frequency select pin.				·	
25       GND       PWR       Ground pin.         26       OE5#       IN       Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs         27       DIF_5       OUT       0.7V differential true clock output         28       DIF_5#       OUT       0.7V differential complement clock output         29       N/C       N/C       No Connection.         30       HIGH_BW#       IN       3.3V input for selecting PLL Band Width 0 = High, 1 = Low         31       FS2       IN       Frequency select pin.					
26     OE5#     IN     Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs       27     DIF_5     OUT     0.7V differential true clock output       28     DIF_5#     OUT     0.7V differential complement clock output       29     N/C     N/C     No Connection.       30     HIGH_BW#     IN     3.3V input for selecting PLL Band Width 0 = High, 1 = Low       31     FS2     IN     Frequency select pin.					
26     0Es#     IN     1 = tri-state outputs, 0 = enable outputs       27     DIF_5     OUT     0.7V differential true clock output       28     DIF_5#     OUT     0.7V differential complement clock output       29     N/C     N/C     No Connection.       30     HIGH_BW#     IN     3.3V input for selecting PLL Band Width 0 = High, 1 = Low       31     FS2     IN     Frequency select pin.	25	GND	PWR		
28       DIF_5#       OUT       0.7V differential complement clock output         29       N/C       N/C       No Connection.         30       HIGH_BW#       IN       3.3V input for selecting PLL Band Width 0 = High, 1 = Low         31       FS2       IN       Frequency select pin.	26	OE5#	IN		
29     N/C     N/C     No Connection.       30     HIGH_BW#     IN     3.3V input for selecting PLL Band Width 0 = High, 1 = Low       31     FS2     IN     Frequency select pin.	27	DIF_5	OUT	0.7V differential true clock output	
30     HIGH_BW#     IN     3.3V input for selecting PLL Band Width 0 = High, 1 = Low       31     FS2     IN     Frequency select pin.	28	DIF_5#	OUT	0.7V differential complement clock output	
30         HIGH_BW#         IN         0 = High, 1= Low           31         FS2         IN         Frequency select pin.	29	N/C	N/C	No Connection.	
31 FS2 IN Frequency select pin.	30	HIGH_BW#	IN	3.3V input for selecting PLL Band Width	
	31	FS2	IN		
32 SMBCLK IN Clock pin of SMBUS circuitry, 5V tolerant	32	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant	

# **Pin Description**

33         SMBDAT         I/O         Data pin of SMBUS circuitry, 5V tolerant           24         FS1         IN         3.3V Frequency select latched input pin.           35         BYPASS#/PLL         IN         Input to select Bypass (fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode           36         VTTPWRGD#/PD         IN         Input to select Bypass (fan-out) or PLL (ZDB) mode           37         DIF_6#         OUT         0.7V differential complement clock output           38         DIF_6         OUT         0.7V differential true clock output           39         OE6#         IN         Active low input for enabling DIF pair 6.           39         OE6#         IN         Active low input for enabling DIF pair 6.           40         GND         PWR         Ground pin.           41         VDD         PVR         Power supply, nominal 3.3V           42         DIF_7#         OUT         0.7V differential complement clock output           43         DIF_7#         OUT         0.7V differential complement clock output           44         OE7#         IN         1 = tri-state outputs, 0 = enable outputs           45         DIF_8         OUT         0.7V differential complement clock output           46         DIF_8	PIN #	PIN NAME	TYPE	DESCRIPTION
35         BYPASS#/PLL         IN         Input to select Bypass (an-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode           36         VTTPWRGD#/PD         IN         allow the device to Power Up. PD is an asynchronous active high input in used to put the device into a low power state. The internal clocks and PLLs are stopped.           37         DIF_6#         OUT         0.7V differential complement clock output           38         DIF_6         OUT         0.7V differential rue clock output           39         OE6#         IN         Active low input for enabling DIF pair 6.           31         I = fristate outputs, 0 = enable outputs         1           40         GND         PWR         Ground pin.           41         VDD         PWR         Power supply, nominal 3.3V           42         DIF_7#         OUT         0.7V differential complement clock output           43         DIF_7#         OUT         0.7V differential complement clock output           44         OE7#         IN         Active low input for enabling DIF pair 7.           45         DIF_8#         OUT         0.7V differential complement clock output           46         DIF_8         OUT         0.7V differential complement clock output           47         OE8#         IN         1 = tri-state outputs, 0 = en	33	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
35     BYPASS#/PLL     IN     0 = Bypass mode, 1 = PLL mode       36     VTTPWRGD#/PD     IN     VTTPWRGD# is an active tow input used to sample latched inputs and allow the device into a low power state. The internal clocks and PLLs are stopped.       37     DIF_6#     OUT     0.7V differential complement clock output       38     DIF_6     OUT     0.7V differential true clock output       39     OE6#     IN     Active low input for enabling DIF pair 6.       40     GND     PWR     Ground pin.       41     VDD     PWR     Power supply, nominal 3.3V       42     DIF_7#     OUT     0.7V differential rue clock output       43     DIF_7     OUT     0.7V differential rue clock output       44     OE7#     IN     Active low input for enabling DIF pair 7.       43     DIF_7#     OUT     0.7V differential rue clock output       44     OE7#     IN     Active low input for enable outputs       45     DIF_8#     OUT     0.7V differential rue clock output       46     DIF_9     OUT     0.7V differential rue clock output       47     OE8#     IN     Active low input for enable outputs       48     VDD     PWR     Ground pin.       50     DIF_9#     OUT     0.7V differential rue clock output	34	FS1	IN	3.3V Frequency select latched input pin.
0         = Bypass mode, 1= PLL mode           36         VTTPWRGD#/PD         IN           37         DIF_6#         OUT         0.7V differential complement clock output           38         DIF_6         OUT         0.7V differential rue clock output           38         DIF_6         OUT         0.7V differential rue clock output           39         OE6#         IN         Active tow input for enabling DIF par 6.           40         GND         PWR         Ground pin.           41         VDD         PWR         Ground pin.           42         DIF_7         OUT         0.7V differential complement clock output           43         DIF_7         OUT         0.7V differential complement clock output           44         OE7#         IN         Active low input for enabling DIF pair 7.           44         OE7#         IN         Active low input for enable outputs           44         OE7#         IN         Active low input for enable outputs           44         OE7#         IN         Active low input for enable outputs           45         DIF_8#         OUT         0.7V differential complement clock output           46         DIF_9         OUT         0.7V differential complement clock output	35	BYPASS#/PLI	IN	
36         VTTPWRGD#/PD         IN         allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.           37         DIF_6#         OUT         0.7V differential complement clock output           38         DIF_6         OUT         0.7V differential true clock output           39         OE6#         IN         Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs           40         GND         PWR         Fower supply, nominal 3.3V           41         VDD         PWR         Power supply, nominal 3.3V           42         DIF_7#         OUT         0.7V differential true clock output           43         DIF_7         OUT         0.7V differential true clock output           44         OE7#         IN         Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs           45         DIF_8#         OUT         0.7V differential complement clock output           46         DIF_8         OUT         0.7V differential complement clock output           47         OE8#         IN         Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs           48         VDD         PWR         Rower supply, nominal 3.3V		BHAGGMILL		
36       VT1PWRGD#/PD       IN       pin used to put the device into a low power state. The internal clocks and PLLs are stopped.         37       DIF_6#       OUT       0.7V differential complement clock output         38       DIF_6       OUT       0.7V differential complement clock output         39       OE6#       IN       Active low input for enabling DIF pair 6.         40       GND       PWR       Ground pin.         41       VDD       PWR       Power supply, nominal 3.3V         42       DIF_7#       OUT       0.7V differential complement clock output         43       DIF_7       OUT       0.7V differential complement clock output         44       OE7#       IN       Active low input for enabling DIF pair 7.         44       OE7#       IN       Active low input for enabling DIF pair 8.         45       DIF_8#       OUT       0.7V differential true clock output         46       DIF       ODD       PWR       Power supply, nominal 3.3V         47       OE8#       IN       Active low input for enabling DIF pair 8.         1 = tri-state outputs, 0 = enable outputs       0       To differential true clock output         50       DIF_9#       OUT       0.7V differential true clock output       0      <				
PLLs are stopped.37DIF_6#OUT0.7V differential complement clock output38DIF_6OUT0.7V differential true clock output39OE6#INActive low input for enable outputs.40GNDPWRGround pin.41VDDPWRPower supply, nominal 3.3V42DIF_7#OUT0.7V differential complement clock output43DIF_7OUT0.7V differential true clock output44OE7#INActive low input for enabling DIF pair 7.45DIF_8#OUT0.7V differential true clock output46DIF_8OUT0.7V differential complement clock output47OE8#INActive low input for enabling DIF pair 8.48VDDPWRPower supply, nominal 3.3V49GNDPWRGround pin.50DIF_9#OUT0.7V differential complement clock output51DIF_9OUT0.7V differential cock output53DIF_9#OUT0.7V differential cock output54DIF_9#OUT0.7V differential cock output55OE9#IN1 = tri-state outputs, 0 = enable outputs54DIF_10#OUT0.7V differential cock output55OE10#IN1 = tri-state outputs, 0 = enable outputs56GNDPWRGround pin.57VDDPWRGround pin.58DIF_11#OUT0.7V differential cock output59OE10#IN <td>36</td> <td>VTTPWRGD#/PD</td> <td>IN</td> <td></td>	36	VTTPWRGD#/PD	IN	
37DIF_6#OUT0.7V differential complement clock output38DIF_6OUT0.7V differential true clock output39OE6#INActive low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs40GNDPWRGround pin.41VDDPWRPower supply, nominal 3.3V42DIF_7#OUT0.7V differential complement clock output43DIF_7OUT0.7V differential cock output44OE7#INActive low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs44OE7#INActive low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs45DIF_8OUT0.7V differential true clock output46DIF_8OUT0.7V differential true clock output47OE8#INActive low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs48VDDPWRGround pin.50DIF_9#OUT0.7V differential true clock output51DIF_9OUT0.7V differential complement clock output53DIF_10#OUT0.7V differential complement clock output54DIF_10OUT0.7V differential true clock output55OE10#INActive low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs54DIF_11#OUT0.7V differential true clock output55OE10#INActive low input for enabling DIF pair 11. 1 = tri-state outputs				
38         DIF_6         OUT         0.7V differential true clock output           39         OE6#         IN         Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs           40         GND         PWR         Ground pin.           41         VDD         PWR         Power supply, nominal 3.3V           42         DIF_7#         OUT         0.7V differential complement clock output           43         DIF_7         OUT         0.7V differential true clock output           44         OE7#         IN         Active low input for enable outputs           44         OE7#         IN         Active low input for enable outputs           45         DIF_8#         OUT         0.7V differential complement clock output           46         DIF_8         OUT         0.7V differential complement clock output           47         OE8#         IN         Active low input for enable outputs           48         VDD         PWR         Power supply, nominal 3.3V           49         GND         PWR         Ground pin.           50         DIF_9#         OUT         0.7V differential complement clock output           51         DIF_9#         OUT         0.7V differential complement clock output	37	DIF 6#	OUT	
39 $OE6\#$ INActive low input for enabling DIF pair 6. 1 = tri-state outputs. 0 = enable outputs40GNDPWRGround pin.41VDDPWRPower supply, nominal 3.3V42DIF_7#OUT0.7V differential complement clock output43DIF_7OUT0.7V differential complement clock output44OE7#INActive low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs45DIF_8#OUT0.7V differential complement clock output46DIF_8OUT0.7V differential complement clock output47OE8#INActive low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs48VDDPWRPower supply, nominal 3.3V49GNDPWRGround pin.50DIF_9#OUT0.7V differential complement clock output51DIF_9OUT0.7V differential complement clock output52OE9#INActive low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs53DIF_10#OUT0.7V differential true clock output54DIF_11#OUT0.7V differential complement clock output55OE10#INActive low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs54DIF_11#OUT0.7V differential complement clock output55OE10#INActive low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs56GNDPWR <td></td> <td></td> <td></td> <td></td>				
40GNDPWRGround pin.41VDDPWRGround pin.42DIF_7#OUT0.7V differential complement clock output43DIF_7OUT0.7V differential true clock output44OE7#IN1 = tri-state outputs, 0 = enable outputs44OE7#IN1 = tri-state outputs, 0 = enable outputs45DIF_8#OUT0.7V differential complement clock output46DIF_8OUT0.7V differential complement clock output47OE8#INActive low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs48VDDPWRPower supply, nominal 3.3V49GNDPWRGround pin.50DIF_9#OUT0.7V differential complement clock output51DIF_9OUT0.7V differential true clock output52OE9#IN1 = tri-state outputs, 0 = enable outputs53DIF_10#OUT0.7V differential complement clock output54DIF_10OUT0.7V differential complement clock output55OE10#IN1 = tri-state outputs, 0 = enable outputs56GNDPWRGround pin.57VDDPWRPower supply, nominal 3.3V58DIF_11#OUT0.7V differential complement clock output60OE11#IN1 = tri-state outputs, 0 = enable outputs58DIF_11#OUT0.7V differential complement clock output60OE11#IN1 = tri-s				
41       VDD       PWR       Power supply, nominal 3.3V         42       DIF_7#       OUT       0.7V differential complement clock output         43       DIF_7       OUT       0.7V differential complement clock output         44       OE7#       IN       Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs         45       DIF_8#       OUT       0.7V differential complement clock output         46       DIF_8       OUT       0.7V differential rue clock output         47       OE8#       IN       Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs         48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential rue clock output         51       DIF_9       OUT       0.7V differential rue clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential rue clock output         54       DIF_10       OUT       0.7V differential complement clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri	39	OE6#	IN	
42DIF_7#OUT0.7V differential complement clock output43DIF_7OUT0.7V differential true clock output44OE7#INActive low input for enable outputs45DIF_8#OUT0.7V differential complement clock output46DIF_8OUT0.7V differential complement clock output47OE8#INActive low input for enable outputs48VDDPWRPower supply, nominal 3.3V49GNDPWRGround pin.50DIF_9#OUT0.7V differential complement clock output51DIF_9OUT0.7V differential complement clock output52OE9#INActive low input for enabling DIF pair 9.53DIF_10#OUT0.7V differential complement clock output54DIF_10#OUT0.7V differential complement clock output55OE10#INActive low input for enabling DIF pair 9.54DIF_10#OUT0.7V differential complement clock output55OE10#INActive low input for enabling DIF pair 10.56GNDPWRGround pin.57VDDPWRPower supply, nominal 3.3V58DIF_11#OUT0.7V differential complement clock output60OE11#INActive low input for enabling DIF pair 10.61FS0IN3.3V Frequency select latched input pin.62IREFOUT0.7V differential complement clock output63AGNDPWR <t< td=""><td>40</td><td>GND</td><td>PWR</td><td>Ground pin.</td></t<>	40	GND	PWR	Ground pin.
43         DIF_7         OUT         0.7V differential true clock output           44         OE7#         IN         Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs           45         DIF_8#         OUT         0.7V differential complement clock output           46         DIF_8         OUT         0.7V differential complement clock output           47         OE8#         IN         Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs           48         VDD         PWR         Ground pin.           50         DIF_9#         OUT         0.7V differential complement clock output           51         DIF_9         OUT         0.7V differential complement clock output           52         OE9#         IN         Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs           53         DIF_10#         OUT         0.7V differential complement clock output           54         DIF_10         OUT         0.7V differential rue clock output           55         OE10#         IN         Active low input for enable outputs           55         OE10#         IN         Active low input for enable outputs           56         GND         PWR         Ground pin.           5	41	VDD	PWR	Power supply, nominal 3.3V
44       OE7#       IN       Active low input for enabling DIF pair 7. 1 = tri-state outputs.         45       DIF_8#       OUT       0.7V differential complement clock output         46       DIF_8       OUT       0.7V differential true clock output         47       OE8#       IN       Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs         48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential true clock output         51       DIF_9       OUT       0.7V differential true clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential true clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Powe	42	DIF_7#	OUT	0.7V differential complement clock output
44       OE/#       IN       1 = tri-state outputs, 0 = enable outputs         45       DIF_8#       OUT       0.7V differential complement clock output         46       DIF_8       OUT       0.7V differential true clock output         47       OE8#       IN       Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs         48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential true clock output         51       DIF_9       OUT       0.7V differential complement clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         55       OE10#       IN       1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         <	43	DIF_7	OUT	0.7V differential true clock output
45       DIF_8#       OUT       0.7V differential complement clock output         46       DIF_8       OUT       0.7V differential rue clock output         47       OE8#       IN       Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs         48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential true clock output         51       DIF_9       OUT       0.7V differential complement clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential true clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential true clock outp	44	OF7#	IN	
46       DIF_8       OUT       0.7V differential true clock output         47       OE8#       IN       Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs         48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential complement clock output         51       DIF_9       OUT       0.7V differential true clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       1 =				
47       OE8#       IN       Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs         48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential complement clock output         51       DIF_9       OUT       0.7V differential true clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Ground pin.         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11#       OUT       0.7V differential complement clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input p				
47       OES#       IN       1 = tri-state outputs, 0 = enable outputs         48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential complement clock output         51       DIF_9       OUT       0.7V differential complement clock output         52       OE9#       IN       Active low input for enabling DIF pair 9.         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential rue clock output         55       OE10#       IN       Active low input for enabling DIF pair 10.         56       GND       PWR       Ground pin.         57       VDD       PWR       Ground pin.         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11       OUT       0.7V differential rue clock output         60       OE11#       IN       Active low input for enabling DIF pair 11.         1       tri-state outputs, 0 = enable outputs       61         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF <td>46</td> <td>DIF_8</td> <td>OUT</td> <td></td>	46	DIF_8	OUT	
48       VDD       PWR       Power supply, nominal 3.3V         49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential complement clock output         51       DIF_9       OUT       0.7V differential true clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential complement clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IR	47	OE8#	IN	
49       GND       PWR       Ground pin.         50       DIF_9#       OUT       0.7V differential complement clock output         51       DIF_9       OUT       0.7V differential true clock output         52       OE9#       IN       Active low input for enabling DIF pair 9.         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential complement clock output         55       OE10#       IN       Active low input for enabling DIF pair 10.         56       GND       PWR       Ground pin.         57       VDD       PWR       Ground pin.         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11       OUT       0.7V differential complement clock output         60       OE11#       IN       Active low input for enabling DIF pair 11.         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       OUT       This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establishe the appropriate current. 475 ohms is the standard value.         63       AGND	40			
50       DIF_9#       OUT       0.7V differential complement clock output         51       DIF_9       OUT       0.7V differential true clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential true clock output         59       DIF_11       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       OUT       This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.         63       AGND       PWR       Analog Ground pin for Core PLL				
51       DIF_9       OUT       0.7V differential true clock output         52       OE9#       IN       Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs         53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       OUT       This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.         63       AGND       PWR       Analog Ground pin for Core PLL				•
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53       DIF_10#       OUT       0.7V differential complement clock output         54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       OUT       This pin establishes the reference current for the differential current- mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.         63       AGND       PWR       Analog Ground pin for Core PLL	52	OE9#	IN	
54       DIF_10       OUT       0.7V differential true clock output         55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       OUT         63       AGND       PWR       Analog Ground pin for Core PLL	53	DIF 10#	OUT	
55       OE10#       IN       Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs         56       GND       PWR       Ground pin.         57       VDD       PWR       Power supply, nominal 3.3V         58       DIF_11#       OUT       0.7V differential complement clock output         59       DIF_11       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       OUT         63       AGND       PWR       Analog Ground pin for Core PLL				· · · ·
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59       DIF_11       OUT       0.7V differential true clock output         60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       OUT         63       AGND       PWR       Analog Ground pin for Core PLL	57	VDD	PWR	Power supply, nominal 3.3V
60       OE11#       IN       Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       This pin establishes the reference current for the differential current- mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.         63       AGND       PWR       Analog Ground pin for Core PLL	58	DIF_11#	OUT	0.7V differential complement clock output
60       OE11#       IN       1 = tri-state outputs, 0 = enable outputs         61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       This pin establishes the reference current for the differential current- mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.         63       AGND       PWR       Analog Ground pin for Core PLL	59	DIF_11	OUT	
61       FS0       IN       3.3V Frequency select latched input pin.         62       IREF       OUT       This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.         63       AGND       PWR       Analog Ground pin for Core PLL	60	OE11#	IN	
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62     IREF     OUT     mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.       63     AGND     PWR     Analog Ground pin for Core PLL	61	FSU	IN	
62     IREF     OUT     ground in order to establish the appropriate current. 475 ohms is the standard value.       63     AGND     PWR     Analog Ground pin for Core PLL				
63     AGND     PWR     Analog Ground pin for Core PLL	62	IREF	OUT	
63 AGND PWR Analog Ground pin for Core PLL				
	63	AGND	PWR	

#### **Absolute Max**

Symbol	Parameter	Min	Max	Units
VDDA	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Supply Voltage		4.6	V
V <sub>IL</sub>	Input Low Voltage	GND-0.5		V
V <sub>IH</sub>	Input High Voltage		$V_{DD}$ +0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	С°
Tcase	Case Temperature		115	°C
	Input ESD protection			
ESD prot	human body model	2000		V

# **Electrical Characteristics - Input/Supply/Common Output Parameters**

 $T_A$  = 0 - 70°C; Supply Voltage  $V_{DD}$  = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V <sub>IH</sub>	3.3 V +/-5%	2		V <sub>DD</sub> + 0.3	V	
Input Low Voltage	V <sub>IL</sub>	3.3 V +/-5%	GND - 0.3		0.8	V	
Input High Current	I <sub>IH</sub>	$V_{IN} = V_{DD}$	-5		5	uA	
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5			uA	
input Low Culterit	$I_{IL2}$	$V_{IN} = 0$ V; Inputs with pull-up resistors	-200			uA	
Operating Supply Current	I <sub>DD3.3OP</sub>	Full Active, C <sub>L</sub> = Full load;		263	350	mA	1
Powerdown Current	I <sub>DD3.3PD</sub>	all differential pairs tri-stated		24	30	mA	1
Input Frequency	F <sub>iPLL</sub>	PLL Mode	100		400	MHz	1
input Frequency	F <sub>iBYPASS</sub>	Bypass Mode	33		400	MHz	1
Pin Inductance	L <sub>pin</sub>				7	nH	1
Capacitance	CIN	Logic Inputs	1.5		5	рF	1
Capacitance	COUT	Output pin capacitance			6	pF	1
PLL Bandwidth	BW	PLL Bandwidth when PLL_BW=0	2	3	4	MHz	1
	DW	PLL Bandwidth when PLL_BW=1	0.7	1	1.4	MHz	1
Clk Stabilization	T <sub>STAB</sub>	From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Modulation Frequency	f <sub>MOD</sub>	Triangular Modulation	30		33	kHz	1
OE# Latency	t <sub>LATOE#</sub>	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,3
Tdrive_PD	t <sub>DRVPD</sub>	DIF output enable after PD de-assertion			300	us	1,3
Tfall	t <sub>F</sub>	Fall time of OE#			5	ns	1
Trise	t <sub>R</sub>	Rise time of OE#			5	ns	2

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>See timing diagrams for timing requirements.

<sup>3</sup>Time from deassertion until outputs are >200 mV

IDT<sup>™</sup>/ICS<sup>™</sup> Twelve Output Differential Buffer for PCIe Gen 1 and Gen 2

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### **Electrical Characteristics - DIF 0.7V Current Mode Differential Pair**

 $T_{A} = 0 - 70^{\circ}C; \ V_{DD} = 3.3 \ V \ \text{+/-5\%}; \ C_{L} = 2pF, \ R_{S} = 33.2\Omega, \ R_{P} = 49.9\Omega, \ R_{REF} = 475\Omega$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo <sup>1</sup>	$V_{O} = V_{x}$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope	660		850	mV	1,3
Voltage Low	VLow	math function.	-150		150	IIIV	1,3
Max Voltage	Vovs	Measurement on single ended			1150	mV	1
Min Voltage	Vuds	signal using absolute value.	-300			111V	1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Rise Time	t <sub>r</sub>	$V_{OL} = 0.175V, V_{OH} = 0.525V$	175		700	ps	1
Fall Time	t <sub>f</sub>	V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V	175		700	ps	1
<b>Rise Time Variation</b>	d-t <sub>r</sub>				125	ps	1
Fall Time Variation	d-t <sub>f</sub>				125	ps	1
Duty Cycle	d <sub>t3</sub>	Measurement from differential wavefrom	45		55	%	1
Skew	t <sub>sk3</sub>	$V_{T} = 50\%$			50	ps	1
Jitter, Cycle to cycle	t.	PLL mode			50	ps	1,5
	t <sub>jcyc-cyc</sub>	BYPASS mode as additive jitter			50	ps	1,5
		PCIe Gen 1 specs (1.5 - 22 MHz)			108	ps	1,6,7
Jitter, Phase	t <sub>jphasePLL</sub>	FBD specs (11-33 MHz)			3	ps rms	1,6,7
		PCIe Gen 2 specs (8-16 MHz, 5-16 MHz)			3.1	ps rms	1,6,7

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements. The 9DB403/803 itself does not contribute to ppm error.

 ${}^{3}I_{REF} = V_{DD}/(3xR_{R})$ . For  $R_{R} = 475\Omega$  (1%),  $I_{REF} = 2.32mA$ .  $I_{OH} = 6 \times I_{REF}$  and  $V_{OH} = 0.7V @ Z_{O} = 50\Omega$ .

<sup>4</sup> Applies to Bypass Mode Only

<sup>5</sup> Measured from differential waveform

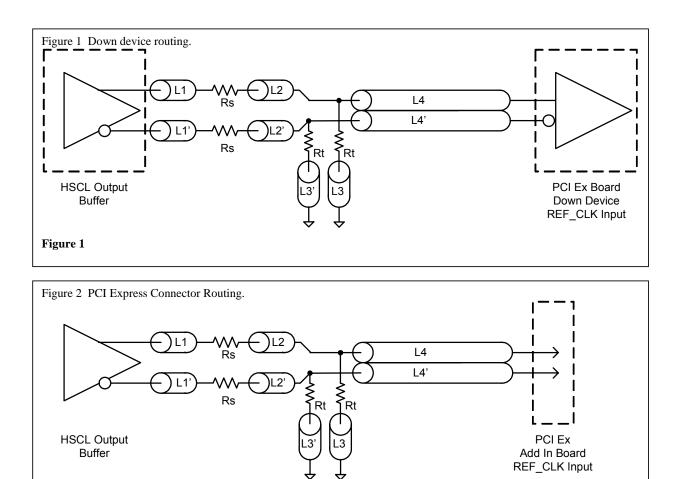
<sup>6</sup> See http://www.pcisig.com for complete specs

<sup>7</sup> Device driven by 932S421BGLF or equivalent

SRC Reference Clock							
Dimension or Value	Unit	Figure					
0.5 max	inch	1					
0.2 max	inch	1					
0.2 max	inch	1					
33	ohm	1					
49.9	ohm	1					
	Dimension or Value0.5 max0.2 max0.2 max33	Dimension or ValueUnit0.5 maxinch0.2 maxinch0.2 maxinch33ohm					

Down Device Differential Routing	Dimension or Value	Unit	Figure
L4 length, Route as coupled <b>microstrip</b> 100 ohm differential trace.	2 min to 16 max	inch	1
L4 length, Route as coupled stripline 100 ohm differential trace.	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector	Dimension or Value	Unit	Figure
L4 length, Route as coupled <b>microstrip</b> 100 ohm differential trace.	0.25 to 14 max	inch	2
L4 length, Route as coupled stripline 100 ohm differential trace.	0.225 min to 12.6 max	inch	2



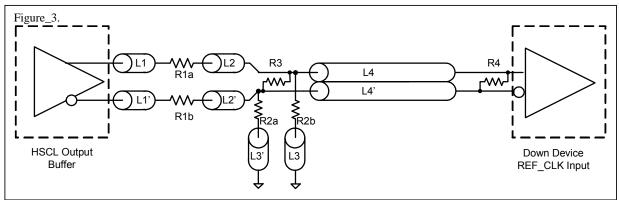
IDT™/ICS™ Twelve Output Differential Buffer for PCIe Gen 1 and Gen 2

Figure 2

Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45 v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS
D1 D11	D 1		1	1			

# Alternative termination for LVDS and other common differential signals. Figure 3.

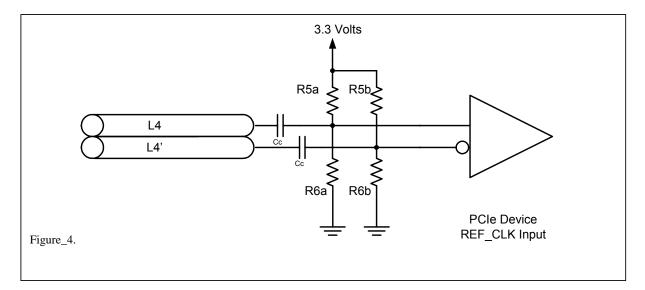
R1a = R1b = R1



R2a = R2b = R2

### Cable connected AC coupled application, figure 4

Component	Value	Note
R5a,R5b	8.2K 5%	
R6a,R6b	1K 5%	
Cc	0.1 uF	
Vcm	0.350 volts	



# General SMBus serial interface information for the ICS9DB1200B

# How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address DC (H)
- ICS clock will acknowledge
- Controller (host) sends the begining byte location = N
- ICS clock will acknowledge
- Controller (host) sends the data byte count = X
- ICS clock will *acknowledge*
- Controller (host) starts sending Byte N through Byte N + X -1
  - (see Note 2)
- ICS clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

# How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address DC (H)
- ICS clock will *acknowledge*
- Controller (host) sends the begining byte location = N
- ICS clock will acknowledge
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address DD (H)
- ICS clock will acknowledge
- ICS clock will send the data byte count = X
- ICS clock sends Byte N + X -1
- ICS clock sends Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8).
- · Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Ind	ex Block W	/rit	e Operation
Cor	ntroller (Host)		ICS (Slave/Receiver)
Т	starT bit		
Slave	e Address DC <sub>(H)</sub>		
WR	WRite		
			ACK
Begi	nning Byte = N		
			ACK
Data	Byte Count = X		
			ACK
Begir	ning Byte N		
			ACK
	$\diamond$	te	
	$\diamond$	X Byte	$\diamond$
	$\diamond$	×	$\diamond$
			$\diamond$
Byte	e N + X - 1		
			ACK
Р	stoP bit		

Ind	ex Block Rea	ad	Operation	
Con	troller (Host)	IC	S (Slave/Receiver)	
Т	starT bit			
Slave	Address DC <sub>(H)</sub>			
WR	WRite			
			ACK	
Begii	nning Byte = N			
			ACK	
RT	Repeat starT			
Slave	Address DD <sub>(H)</sub>			
RD	ReaD			
			ACK	
		Data Byte Count = X		
	ACK			
			Beginning Byte N	
	ACK			
		\te	0	
	0	X Byte	0	
0			0	
	0			
			Byte N + X - 1	
N	Not acknowledge			
Р	stoP bit			

#### SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)

Byte	e 0	Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7		-	HIGH_BW#	High or Low BW	RW	High BW	Low BW	Latch
Bit 6		-	BYPASS#/PLL	Bypass (non-PLL Mode) or PLL Mode	RW	Bypass	PLL	Latch
Bit 5		-	Reserved	Reserved	RW	Rese	erved	Х
Bit 4		-	Reserved	Reserved	RW	Rese	erved	Х
Bit 3		-	Reserved	Reserved	RW	Reserved		Х
Bit 2		-	FS2	Frequency Select 2	RW			Latch
Bit 1	t <b>1</b> - FS1		FS1	Frequency Select 1	RW See F		S Table	Latch
Bit 0		-	FS0	Frequency Select 0	RW	]		Latch

#### SMBus Table: Output Control Register

Byt	e 1	Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7	42	2,41	DIF_7	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 6	38	,37	DIF_6	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 5	34	,33	DIF_5	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 4	30	,29	DIF_4	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 3	20	,21	DIF_3	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 2	16	i,17	DIF_2	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 1	12	.,13	DIF_1	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 0	8	s,9	DIF_0	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1

#### SMBus Table: Output Control Register

Byte	e 2	Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7		-	Reserved	Reserved	RW	Rese	erved	0
Bit 6		-	Reserved	Reserved	RW	Rese	erved	0
Bit 5		-	Reserved	Reserved	RW	Rese	erved	0
Bit 4		-	Reserved	Reserved	RW	Rese	erved	0
Bit 3	58	3,59	DIF_11	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 2	53	3,54	DIF_10	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 1	50	),51	DIF_9	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 0	45	5,46	DIF_8	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1

#### SMBus Table: Output Enable Readback

Byt	e 3	Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7	42	2,41	OE7#	OE# Pin Readback	R	Enabled	Disabled	Х
Bit 6	38	3,37	OE6#	OE# Pin Readback	R	Enabled	Disabled	Х
Bit 5	34	I,33	OE5#	OE# Pin Readback	R	Enabled	Disabled	Х
Bit 4	30	),29	OE4#	OE# Pin Readback	R	Enabled	Disabled	Х
Bit 3	20	),21	OE3#	OE# Pin Readback	R	Enabled	Disabled	Х
Bit 2	16	6,17	OE2#	OE# Pin Readback	R	Enabled	Disabled	Х
Bit 1	12	2,13	OE1#	OE# Pin Readback	R	Enabled	Disabled	Х
Bit 0	8	3,9	OE0#	OE# Pin Readback	R	Enabled	Disabled	Х

#### SMBus Table: Output Enable Readback

Byte	e 4	Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7		-	Reserved	Reserved	R	Rese	erved	0
Bit 6		-	Reserved	Reserved	R	Rese	erved	0
Bit 5		-	Reserved	Reserved	R	Rese	erved	0
Bit 4		-	Reserved	Reserved	R	Rese	erved	0
Bit 3	58	3,59	OE11#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	Х
Bit 2	53	3,54	OE10#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	Х
Bit 1	50	),51	OE9#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	Х
Bit 0	45	5,46	OE8#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	Х

Note: For an output to be enabled, BOTH the Output Enable Bit and the OE# pin must be enabled. This means that the Output Enable Bit must be '1' and the corresponding OE# pin must be '0'.

#### SMBus Table: Vendor & Revision ID Register

Byte	5 Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	Х
Bit 6	-	RID2		R	-	-	Х
Bit 5	-	RID1	REVISIONID	R	-	-	Х
Bit 4	-	RID0		R	-	-	Х
Bit 3	-	VID3		R	-	-	0
Bit 2	-	VID2	VENDOR ID	R	-	-	0
Bit 1	-	VID1	VENDORID	R	-	-	0
Bit 0	-	VID0		R	-	-	1

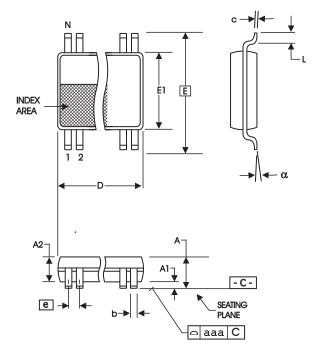
#### SMBus Table: DEVICE ID

Byte	e 6	Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7	-	-		Device ID 7 (MSB)	RW			0
Bit 6	-	-		Device ID 6	RW			0
Bit 5	-	-		Device ID 5	RW			0
Bit 4	-	-		Device ID 4	RW		is 0C Hex	0
Bit 3	-	-		Device ID 3	RW		IS UC Hex	1
Bit 2	-	-		Device ID 2	RW			1
Bit 1	-	-		Device ID 1	RW			0
Bit 0	-	-		Device ID 0	RW			0

#### SMBus Table: Byte Count Register

Byte 7	Pin #	Name	Control Function	Туре	0	1	PWD
Bit 7	-	BC7		RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4	Writing to this register configures how	RW	-	-	0
Bit 3	-	BC3	many bytes will be read back.	RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

ICS9DB1200B REV A 03/21/07



	(240 mil)	(20 mil)			
	In Milli	meters	In Inches		
SYMBOL	COMMON D	IMENSIONS	COMMON D	IMENSIONS	
	MIN	MAX	MIN	MAX	
A		1.20		.047	
A1	0.05	0.15	.002	.006	
A2	0.80	1.05	.032	.041	
b	0.17	0.27	.007	.011	
С	0.09	0.20	.0035	.008	
D	SEE VAF	RIATIONS	SEE VAF	RIATIONS	
E	8.10 E	BASIC	0.319 BASIC		
E1	6.00	6.20	.236	.244	
е	0.50 E	BASIC	0.020	BASIC	
L	0.45	0.75	.018	.030	
N	SEE VARIATIONS		SEE VAF	IATIONS	
α	0°	8°	0°	8°	
aaa		0.10		.004	

6.10 mm. Body, 0.50 mm. Pitch TSSOP

#### VARIATIONS

N	Dr	nm.	D (inch)		
IN	MIN	MAX	MIN	MAX	
64	16.90	17.10	.665	.673	

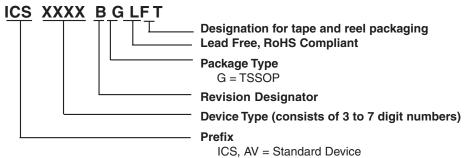
Reference Doc.: JEDEC Publication 95, MO-153

10-0039

# **Ordering Information**

### ICS9DB1200BGLFT

Example:



#### **Revision History**

Rev.	Issue Date	Description	Page #
		1. Updated IDD characteristics.	
А	06/21/07	2. Release to Final.	5

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